Design of Analog Integrated Circuits Immune to RFI

POLITECNICO DI TORINO

SCUOLA DI DOTTORATO
Dottorato in Ing. Elettronica e delle Comunicazioni – XVI ciclo

Tesi di Dottorato

Design of Analog Integrated Circuits Robust to RF Interference

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Febbraio 2004

ʾΕὰν μὴ ἔλπηται, ἀνέλπιστον οὐκ ἐξευρήσει
ʿΗράκλειτος

Summary

This work is aimed to provide analysis tools and criteria which can be employed in the design of analog integrated circuits robust to Electromagnetic Interference (EMI). To this purpose, the nonlinear effects which are induced by EMI in the operation of analog circuits are investigated and related to design parameters and parasitic elements.

In particular, the effects of Radio-Frequency interference (RFI) which is superimposed onto the input voltages and/or onto the power supply rails of opamp-based analog circuits are considered. To this purpose, a two-input Volterra series model, which is suitable to the prediction of distortion induced by RFI superimposed onto the input terminals of opamp-based circuit, and a three-input Volterra series model, which is suitable to the prediction of the effects of RFI superimposed both onto the opamp input voltages and onto the power supply rails, are proposed. Furthermore, a numerical large-signal model which has been proposed in the literature by Fiori is extended in order to provide closed-form prediction of the RFI-induced phenomena in opamp circuits under large-signal EMI excitation.

On the basis of these analysis tools, the relation between opamp configuration, opamp parameters, parasitic elements and susceptibility to EMI is highlighted and the main issues in the design of opamp circuits robust to EMI are discussed. Moreover, an opamp input stage which is intrinsically robust to EMI is presented and its operation principle is discussed on the basis of the models of RFI-induced distortion phenomena in opamp circuits which have been proposed.

Acknowledgments

A special thank to Franco Fiori, both for his valuable contribution to the research activities which have been carried out within the Microelectronics EMC Group during my PhD course and for his constant advice and support.

I would also thank all the colleagues and friends of the Politecnico di Torino and, in particular, of the Microelectronics EMC Group, who shared with me both the delights and the troubles of the last three years.

Finally, I would acknowledge the support of STMicroelectronics (Castelletto Site), which has made possible the physical realization of the integrated circuits presented in this work.

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Chapter 1

Introduction

The most recent achievements of silicon CMOS technology in terms of geometrical scaling and versatility have paved the way to the low cost integration of high performance electronic systems on a single chip (System on a Chip, SoC) and have brought about new challenges in present day microelectronic design.

The fully integration on a single chip of complex systems which include digital, analog, power and RF sections, however, requires a completely new approach in integrated circuit (IC) design [1, 2, 3, 4]. In fact, while traditional IC design is mainly addressed to the optimization in terms of performance of each single function, SoC design should be firstly aware of the overall system integration and of the final application environment. To this purpose, new requirements and new design tradeoffs arise.

The aspects related to chip-level Electromagnetic Compatibility (EMC) [5], i.e. with the adverse effects which may be induced by the unintentional generation, propagation and reception of electromagnetic energy within an integrated circuit, deserve a special attention in complex SoC design. These aspects cover both the adverse effects which are induced in IC operation by electromagnetic energy collected from the external environment (inter-EMC, susceptibility), the adverse effects which may by induced in the external environment by IC operation (inter-EMC, emission) and the adverse effects which are induced by IC operation in different sections within the same IC (intra-EMC).

The susceptibility of IC cells to Radio-Frequency Interference (RFI), in particular, has proven to be among the major threats to SoC reliable operation in both intra-EMC and inter-EMC aspects. In fact, with reference to the typical SoC configuration shown in Fig.1.1, it can be observed that potential sources of interference as high-frequency synchronous digital circuits, RF power amplifiers and switching power supplies are located very close to susceptible circuitry and RF disturbances can easily couple with nominal signal paths through on-chip metal interconnections, I/O pads or via the silicon substrate.

Furthermore, due to the widespread diffusion of wireless integrated systems, which is fostered by the availability of low cost RF systems on silicon, the level of environmental electromagnetic pollution is always increasing. As a consequence, an always increasing level of Electromagnetic Interference (EMI) is collected by wiring structures (cables, PCB traces, bondwires, etc...) in electronic systems from the outside environment and it is translated into RF voltages and currents superimposed onto SoC nominal signals. For instance, an RF incident field with a frequency of 900MHz and a peak amplitude of 10V/m, which is a common value in the proximity of a cell phone antenna, can induce on a PCB trace of 10cm, which acts as an electrical dipole, an RF voltage as high as 1Vpk.

Finally, the threats related to the susceptibility to RFI become more and more severe in low voltage design. In fact, the reduction of IC power supply voltages which is imposed by geometrical scaling and by low power constraints makes the amplitude of RF interference very often comparable with the amplitude of ICs nominal signals or even larger, thus strongly reducing the Signal-to-Noise Ratio (SNR) within a chip.

In conclusion, in order to be suitable to present day SoC challenges, an IC must be designed to operate properly even in the presence of RF interference with a magnitude comparable with nominal signals. In this work, the fulfilment of this requirement with reference to analog ICs, which should provide accurate continuous time, continuous amplitude waveforms, is addressed.

1.1 RFI in Analog Integrated Circuits

Analog integrated circuits, in which the information is carried by continuous time, continuous amplitude voltage or current waveforms, have proven to be very susceptible to RFI. In fact, the RF disturbances which are superimposed onto nominal voltages and currents of an analog circuit are demodulated by the nonlinear characteristics of the active devices (MOS and BJT transistors) which are included in it, the demodulated RFI is added to the nominal output waveforms and their original information content is corrupted [6, 7, 8]. Demodulation of RFI is particularly hazardous because it converts out-of-band high frequency interference into in-band low frequency interference, which cannot be separated from nominal signals through linear filtering. In particular, in the presence of continuous wave (CW) RFI, the output voltage of analog circuits is affected by a DC offset.

In standard analog circuits, the amount of in-band error which is due to the demodulation of out-of-band RFI is very often much higher than the nominal level of accuracy of these circuits. With reference to the widely employed CMOS Miller Opamp circuit connected in the voltage follower configuration shown in Fig.1.2, which operates from a 5V power supply, the amount of the measured RFI-induced DC offset voltage shift is plotted in Fig.1.3 versus the peak amplitude of CW RFI

superimposed onto the input voltage for different RFI frequencies. It can be observed that the RFI-induced offset voltage is comparable with the peak amplitude of CW RFI, therefore, even for relatively small levels of RFI (e.g. 10mVpk), the RFI-induced offset voltage is higher than the typical offset voltage due to transistor mismatch which is usually below 1mV for this circuit topology.

In Fig.1.4 the schematic of a Kujik bandgap voltage reference, which operates from a 5V power supply, is presented. This circuit, that is another widely employed analog building block, is designed to provide a very accurate temperature-independent voltage reference of about 1.2V. The required accuracy of the reference voltage over temperature is very often better than 1mV of residual thermal drift in a temperature range between $-40°C$ and $+120°C$, i.e. few part per million per degree. In Fig.1.5 it can be observed how RFI can severely impair the performance of this circuit. In particular, it can be observed that CW RFI with a frequency of 300MHz and with a peak amplitude of about 10mV superimposed onto the power supply voltage of this circuit is sufficient to induce an error in the output voltage that is significatively higher than the required accuracy over temperature. Furthermore, it can be observed that a CW RFI with a peak amplitude of about 300mV is enough to induce a complete failure in the bandgap voltage reference operation.

The above examples show that analog integrated circuits can be particularly susceptible to RFI and their performance in terms of accuracy can be completely impaired by RFI with a relatively small peak amplitude. Because of the higher and higher degree of interdependence in complex integrated systems, a failure in analog circuit operations can induce an overall system failure which may be destructive. It follows that conventional analog cells are not suitable to present day SoC design and the analog IC design flow should be properly revised in order to achieve immunity to RFI.

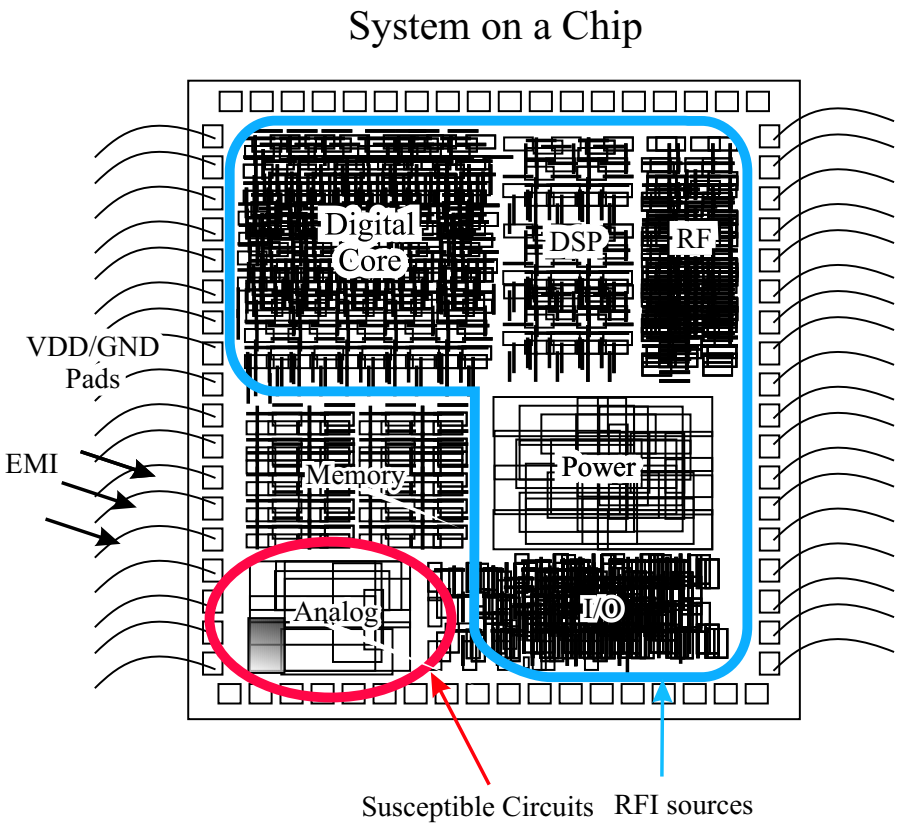


Figure 1.1. Sources of RFI in a present-day System on a Chip (SoC) typical architecture.

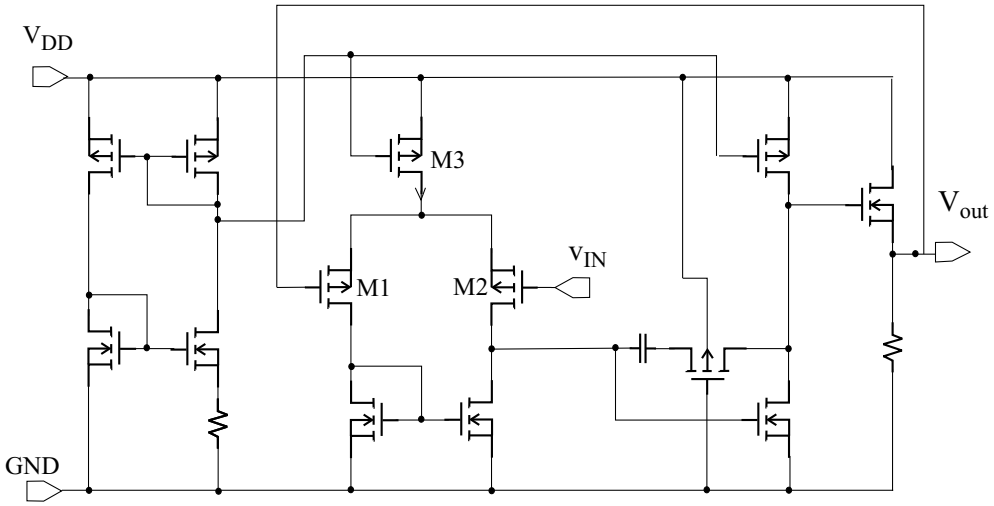


Figure 1.2. CMOS Miller Opamp.

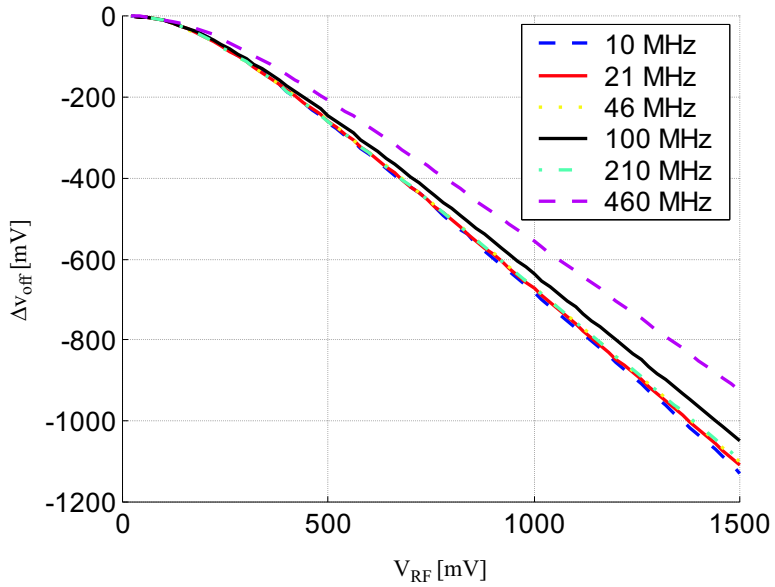


Figure 1.3. CMOS Miller Opamp Susceptibility to EMI.

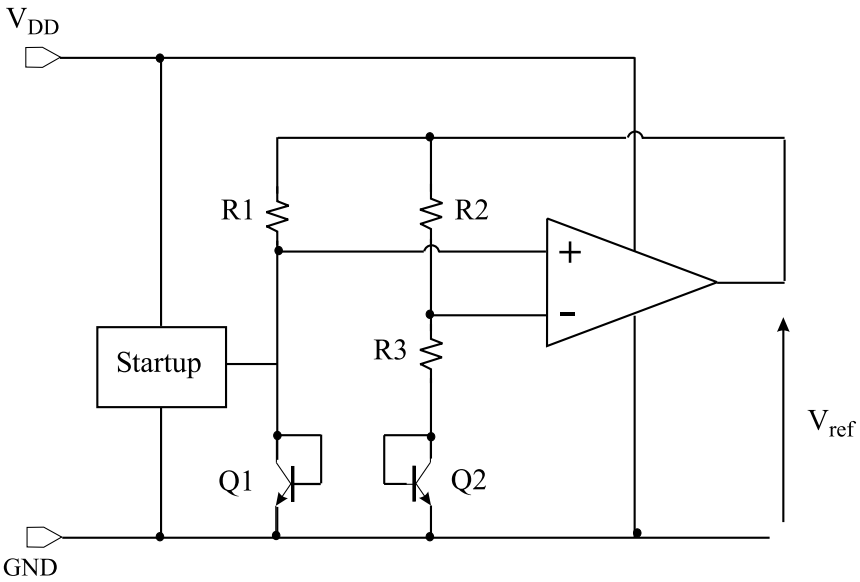


Figure 1.4. Kujik bandgap voltage reference.

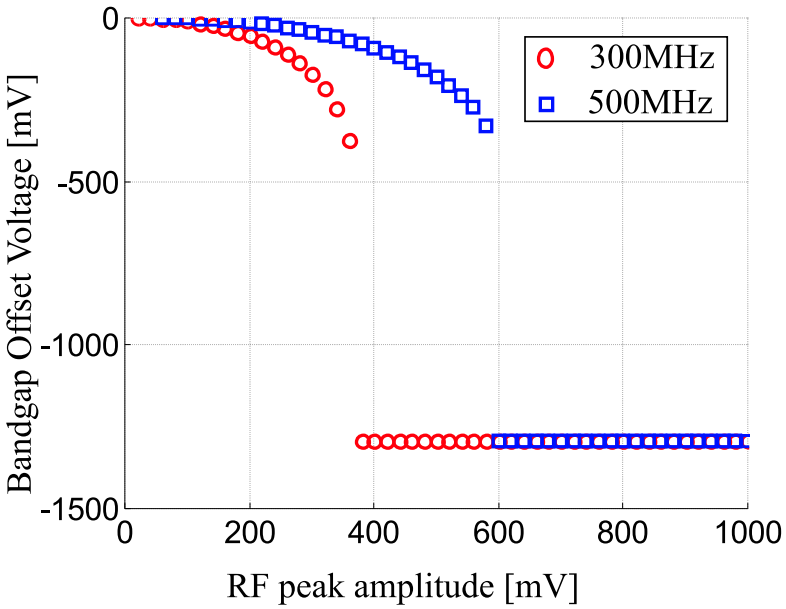


Figure 1.5. Kujik bandgap voltage reference susceptibility to EMI.

1.2 RFI Aspects in Analog IC Design Flow

The susceptibility to RFI is not considered in a standard analog IC design flow. According to a standard design flow (Fig. 1.6a), in fact, an IC is first designed and simulated to achieve a target performance, then it is laid out in order to reduce the occupancy of silicon area and finally it is diffused on silicon. The aspects which are related to the susceptibility to RFI are only considered when the chip or, more often, the overall system in which it operates, fails either in EMI susceptibility compliance tests or in the field. At this point, the problem could only be addressed adding expensive external and/or on-chip shielding and filtering structures which may also adversely affect system performance.

In the last years, EMI immunity aspects have been taken into account earlier in the design flow by post-layout computer simulations which may predict the susceptibility to EMI of a chip before it is actually integrated on silicon (Fig. 1.6b). To this purpose, RFI-oriented models of nonlinear active devices [6, 7, 8], analog circuit macromodels [9, 10, 11, 12, 13, 14, 15, 16, 17, 18] and parasitic extraction tools [19] have been proposed in the literature and implemented in the last years.

These computer-aided techniques let to modify an analog IC design in the first stages in order to enhance its immunity to EMI, nonetheless, they do not provide any tool to design integrated circuits immune to EMI as they only provide information on the susceptibility of a particular design and do not give insight on the origin of the susceptibility to EMI which could be translated into design criteria to enhance the immunity of an analog IC.

In order to face the problems related to the susceptibility to EMI of analog circuits in an effective way, a new, EMI-susceptibility aware design flow is required (Fig. 1.6c). To this purpose, in particular, it is essential to know how the susceptibility to EMI is related to design parameters and parasitics. On the basis of this information, it is possible to take into account the immunity to EMI as an IC specification which can be traded off with other system requirements in the early stage of design.

An EMI-aware analog IC design requires some analysis and design tools: to this purpose, in particular, the behavior of analog integrated circuits in the presence of RF interference should be predicted by an analytical model, which relates in a simple way the susceptibility to RFI to design parameters and parasitic elements. The insight in the operation of analog IC in the presence of RFI which can be gained from such a model, in fact, can be exploited in order to derive design criteria to improve the immunity to RFI of standard analog cells and to design new high-immunity building blocks for specific analog functionalities.

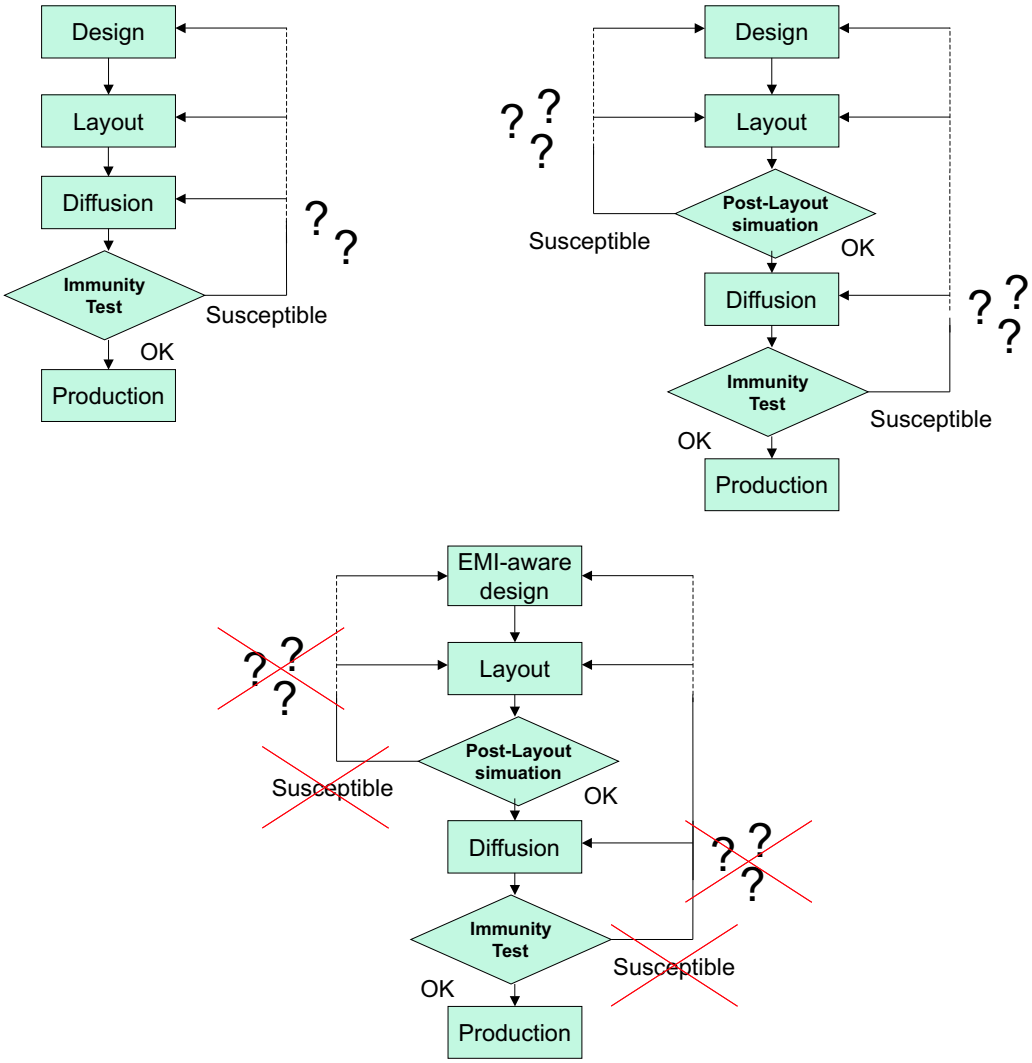


Figure 1.6. RFI Aspects in Analog IC Design Flows.

This work is aimed to provide some of the tools which are required in the design of analog integrated circuits robust to EMI. In Chapter II, in particular, the aspects related to the nonlinear effects of RFI in analog ICs are generally considered and the main techniques which are employed in the analysis of nonlinear electronic circuits and systems are shortly revised in order to highlight the advantages and the drawbacks of these techniques in the investigation of the effects of EMI in analog circuits.

In Chapter III the analytical modelling of the susceptibility to EMI of operational amplifiers is dealt with. In particular, two Volterra series analytical models which are suitable to predict the behavior of integrated opamp circuits in the presence of RFI superimposed onto nominal signals and/or onto the power supply voltages are proposed and these models are validated by experimental tests. Furthermore, the numerical model which has been proposed by Fiori in [20] for the prediction of the RFI-induced offset voltage in opamp circuits under large-signal excitation is extended. In particular, a closed-form expression of the RFI-induced offset voltage is derived and the dependence on RFI frequency of the RFI-induced offset is highlighted.

In Chapter IV, the analytical tools which have been proposed are employed in order to derive design criteria to enhance the immunity to EMI of opamp circuits. To this purpose, the influence of the feedback configuration in the susceptibility to EMI of opamp circuits is discussed, the dependence of the intrinsic susceptibility to EMI of IC opamps on design parameters and parasitic elements is highlighted and the design tradeoffs which should be considered in order to enhance the immunity to EMI are discussed. Furthermore, in Chapter IV a new opamp topology which has been designed to achieve a high immunity to EMI is presented and its operation principle is discussed. Moreover, the extension of the high immunity design criteria, which have been proposed, to analog circuits and subsystems is considered.

Finally, in Chapter V, the main results which have been obtained in this research are summarized, the topics which deserve further investigations are focused and some concluding remarks are drawn.

Chapter 2

Nonlinear Effects of RFI in Analog Integrated Circuits

A good insight in the mechanisms, which are responsible of the EMI-induced failures in analog ICs, and the availability of analysis tools, which could effectively and efficiently predict the behavior of analog ICs in the presence of EMI, are key issues in EMI-aware analog circuit design.

The main task of EMI-aware analog circuit analysis, in particular, is to highlight how out-of-band interference affects the in-band operation of analog integrated circuits. To this purpose, it should be observed that linear time invariant (LTI) systems cannot transfer the power of their input signals from one region of the spectrum to another as, in the most general case, any output of a linear system is given by a complex, frequency-dependent, linear combination of the input signals. As a consequence, the adverse effects which are induced by RFI in analog IC operation are necessarily related to high-frequency *nonlinear phenomena* therefore, RFI-oriented analog circuit modelling requires a proper modelling of nonlinear phenomena.

This Chapter is aimed to provide the basic concepts of nonlinear circuit theory and the fundamental insight in nonlinear circuit analysis techniques which are suitable to the investigation of the nonlinear effects of RFI in analog integrated circuits. In particular, the potential advantages and limitations of each nonlinear analysis technique with reference to the above mentioned investigations will be highlighted.

The general concepts and results which are presented in this Chapter are derived from [21, 22, 23], where a comprehensive presentation of nonlinear circuit theory and analysis can be found.

2.1 Susceptibility to RFI and Harmonic Distortion

The phenomena which are responsible of the susceptibility to RFI of analog circuits are strictly related to *harmonic distortion*, i.e. with the parasitic nonlinear effects that occur in electronic circuits which are designed to be linear. The term *harmonic distortion* refers to the effect of nonlinearity in the frequency-domain analysis of dynamical systems: while in non-autonomous LTI systems the harmonic content of input signals is conserved (i.e., the spectrum of any output signal includes the same harmonic components included in the input signals and the LTI system only affects the amplitude and phase of each spectral component), nonlinear systems may generate spectral components which are not included in the input signals.

In particular the term *harmonic distortion* refers to the generation of distortion terms at frequencies which are expressed by an integer linear combination of the frequencies of input signals, i.e., if the input signals include harmonic components with frequencies ω_1,ω_2,...,ω_i, an output signal may include, in the most general case, spectral components at any frequency

$$\omega = k_1\omega_1 + k_2\omega_2 + \ldots + k_i\omega_i,$$

where $k_1,\ldots,k_i \in \mathbf{Z}$. Spectral components in which there is only one nonzero k_i coefficient are referred to as *harmonics* of the input signals, while spectral components in which there are two or more nonzero k_i coefficients are referred to as *intermodulation products*.

Nonlinear systems whose operation can be completely described in terms of harmonic distortion are referred to as *weakly nonlinear systems*, while the remaining nonlinear systems are referred to as *strongly nonlinear systems*. Strongly nonlinear systems, in particular, may show nonlinear phenomena as sub-harmonic generation, sensible dependence on initial conditions, multiple steady-state behavior and chaotic behavior [22]. In these systems, the output spectrum may include sub-harmonics (i.e. harmonics of fractional order) of the input signals or can be apparently not related to the input signal spectrum at all.

The nonlinear effects which are induced by RFI in analog integrated circuits can be usually considered as a perturbation from the nominal linear circuit operation, therefore they are conveniently described in terms of harmonic distortion. For this reason, harmonic distortion in *weakly nonlinear systems* will be considered hereafter.

2.1.1 Classification and Effects of Harmonic Distortion

Harmonic distortion in systems which are designed to be linear is usually described in terms of the power series expansion of the static nonlinear characteristics which induce distortion:

$$f(x) = y_0 + \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 + \dots . \tag{2.1}$$

With reference to this expansion, y_0 describes the output of the system if no input signal is applied (*bias point* term), the term $\alpha_1 x$ describes the nominal linear operation of the system (linear term or small-signal term) while the terms $\alpha_m x^m$ $(m > 1)$ are referred to as m-th order distortion terms.

From (2.1), the generation of even-order or odd-order distortion terms can be directly related to the nonlinear characteristics and/or to the structure of a nonlinear system. In particular, it should be observed that a nonlinear characteristic which is an even function in the input signal, i.e.

$$f(x) = f(-x) \qquad \forall x,$$

may only generate even-order distortion terms, while a nonlinear characteristics which is an odd function of the input signals,

$$f(-x) = -f(x) \qquad \forall x$$

may only generate odd-order distortion. In particular, from the last condition, it can be derived that the output signal of fully balanced systems, i.e. systems whose output signal can be expressed as the difference between two identical functions of the input signal and its complement, i.e.

$$f(x) = g(x) - g(-x),$$

where $g(x)$ is an arbitrary nonlinear function, do not generate even-order distortion as, in this special case $f(x)$ is an odd function.

Furthermore, the concept of *order of distortion* is particularly expressive in the frequency domain analysis of weakly nonlinear system because it is closely related to the generation of harmonic content. In particular, it can be shown that if the input signals include harmonic components with frequencies ω_1,ω_2,$\dots$,ω_i, m-th order $(m > 2)$ distortion generates spectral components with angular frequency

$$\omega = k_1\omega_1 + k_2\omega_2 + \dots + k_i\omega_i,$$

with $k_1,\dots,k_i \in \mathbf{Z}$ and

$$\sum_{i=0}^{+\infty} |k_i| = m. \tag{2.2}$$

Moreover, the distinction between even-order and odd-order order distortion terms is particularly meaningful because these two kinds of distortion affect the operation of electronic circuits in different ways and, depending on the application, the effect of odd or even distortion can be either particularly harmful or negligible. It is well known in the literature [21], for instance, that odd order and especially third order distortion is particularly harmful in wide-band RF amplifiers, as this kind of distortion can mix the power of adjacent channels, while even-order distortion is a minor threat as it does not interfere with the operation of an RF amplifier in its nominal signal bandwidth.

On the basis of the above considerations, it is significative to highlight the different effects of even-order and odd-order distortion in the operation of baseband analog integrated circuits in the presence of RFI. To this purpose, the result of second-order and third-order distortion on a two-tone signal, which shows an in-band signal component with frequency ω_{s} and an out-of-band CW RFI component at frequency ω_{RFI} is compared.

In this case, according with (2.2), second-order nonlinearity generates distortion terms at the following frequencies

$$\begin{aligned}
&\omega_{\mathrm{RFI}} - \omega_{\mathrm{RFI}} = 0,\\
&\omega_{\mathrm{s}} - \omega_{\mathrm{s}} = 0,\\
&2\omega_{\mathrm{s}},\\
&2\omega_{\mathrm{RFI}},\\
&\omega_{\mathrm{RFI}} - \omega_{\mathrm{s}},\\
&\omega_{\mathrm{RFI}} + \omega_{\mathrm{s}},
\end{aligned}$$

while third-order nonlinearity generates terms with frequency

$$\begin{aligned}
&\omega_{\mathrm{s}} + \omega_{\mathrm{RFI}} - \omega_{\mathrm{RFI}} = \omega_{\mathrm{s}},\\
&\omega_{\mathrm{RFI}} + \omega_{\mathrm{s}} - \omega_{\mathrm{s}} = \omega_{\mathrm{RFI}},\\
&\omega_{\mathrm{RFI}} + 2\omega_{\mathrm{s}},\\
&\omega_{\mathrm{RFI}} - 2\omega_{\mathrm{s}},\\
&3\omega_{\mathrm{RFI}},\\
&3\omega_{\mathrm{s}}.
\end{aligned}$$

In particular, it can be observed that third order nonlinearity generates in-band contributions at frequency $3\omega_{\mathrm{s}}$ and ω_{s}. The first term is related to the distortion of the in-band signal and it is not related to RFI, while the second term affects the linear in-band amplification and may induce either compression or expansion phenomena [21], i.e. a decrease or an increase in the nominal amplification (attenuation) of the baseband signal, which depends on the amplitude of RFI. This phenomenon is

not considered a major threat in baseband electronic circuit operation, because the RFI-induced fluctuations are usually very small if compared to the nominal value of nominal amplification (attenuation) parameters. Furthermore, electronic circuits are usually designed in order to be insensitive to the absolute values of amplification parameters of nonlinear devices.

Second-order nonlinearity, instead, generates an in-band distortion term with frequency $2\omega_s$ and a DC term $\omega_s - \omega_s = 0$, which are not related to RFI, and a DC term ($\omega_{RFI} - \omega_{RFI} = 0$), which depends on the presence of RFI. Most of the unwanted phenomena that are induced by RFI in analog circuits are related to this last term. An example of the effects of second order distortion is the RFI-offset voltage generation, which has been previously described with reference to Fig.1.3 and Fig.1.5. The same kind of distortion is also responsible of the demodulation of modulated RFI in analog integrated circuits.

The results which have been derived for second-order and third-order distortion can be generalized to even-order and odd-order distortion and let to conclude that in-band operation of analog circuits is affected by out-of-band RF interference mainly because of the effects of even-order distortion. As a consequence, the analysis of the effects of RFI on analog ICs operation should be mainly focused on high-frequency even-order nonlinear effects. This consideration, in particular, will be exploited in the following Chapter in the derivation of simplified nonlinear circuit models which are customized to RFI susceptibility investigations.

2.2 Nonlinear Circuit Analysis

In the previous Section a qualitative description on the nature of the nonlinear phenomena which should be considered in the analysis of the susceptibility to EMI of analog ICs has been presented. In this Section, a review of the nonlinear circuit analysis techniques which can be employed to this purpose is provided and the advantages and limitations of each single technique are highlighted.

A nonlinear circuit analysis technique is any computer-aided or pen-and-paper technique which can express any electrical quantity y (voltage or current) of an electric network in terms of the values of its external excitations e and of the constitutive relations of the devices which are included in it.

From circuit theory, in particular, in any non-degenerated lumped parameter electric network, any electrical quantity (voltage or current) can be expressed as

$$y(t) = G(\mathbf{x}(t),\mathbf{e}(t)) \tag{2.3}$$

where $\mathbf{x}(t)$ is the state vector which include capacitor voltages and inductor currents, $\mathbf{e}(t)$ is the source vector which includes the voltage and current waveforms of independent voltage/current sources and $G : \mathbf{R}^n \rightarrow \mathbf{R}$ is a generic function. Furthermore, the state vector $\mathbf{x}(t)$ satisfies a system of nonlinear ordinary differential equations (ODEs):

$$\dot{\mathbf{x}}(t) = \mathbf{F}(\mathbf{x}(t),\mathbf{e}(t)) \tag{2.4}$$

where $\mathbf{F} : \mathbf{R}^n \rightarrow \mathbf{R}^m$ is a generic vector function. Therefore, any output of an electric circuit can be obtained from (2.3)on the basis of the source vector $\mathbf{e}(t)$ and of the initial state vector $\mathbf{x}(0)$.

The different approaches in nonlinear circuit analysis differ on the techniques which are employed in the solution of the nonlinear ODE (2.4). These techniques can be classified into *time-domain* and *frequency domain* or *steady-state* techniques and will be shortly presented in the following.

2.2.1 Time-Domain Nonlinear Analysis Techniques

Time-domain nonlinear analysis techniques are based on the solution of (2.4) and (2.3) in the time domain. As there is no general expression for the solution of (2.4) when $\mathbf{F}$ is a nonlinear function, such analysis can be performed either numerically by the discretization of (2.4) or by the piecewise linear approximation of $\mathbf{F}$. Both these techniques will be described in the following.

Transient Simulation

The most common approach in time-domain circuit analysis, which is employed in SPICE-like circuit simulation programs for transient analysis, is the numerical solution of the ODE (2.4) through time discretization. In particular, N time samples of the state and input variables are considered and the differential system (2.4) is transformed into a nonlinear algebraic system

$$\hat{F}_i(\mathbf{x}(T_0),\ldots,\mathbf{x}(T_N),\mathbf{e}(T_0),\ldots,\mathbf{e}(T_N)) = 0 \qquad i = 1,\ldots,N \tag{2.5}$$

by approximating derivatives with finite increments. The resulting algebraic nonlinear system, whose unknowns are the time samples $\mathbf{x}(T_0),\ldots,\mathbf{x}(T_N)$ of the state vector, is then solved by an iterative method (typically the Newton-Raphson method or its variants [24]).

Different ODE integration methods differ from the techniques which are employed in the sampling (fixed or variable step), in the discretization of the derivatives (one-step or multi-step methods, implicit or explicit methods) and in the iterative scheme which is employed to solve the nonlinear algebraic system. More details on the particular implementations can be found in [23, 24]. The choice of a particular numerical technique is related to the nonlinear circuit under consideration in order to achieve the best trade-off in terms of accuracy and efficiency. Most high-end circuit simulators provide a wide choice of integration algorithms which can be customized to the circuit under analysis [25, 26].

Time-domain transient simulation, if accurate models for active devices are available and if the values of the parasitic elements are properly extracted by post-layout back-annotation, provides probably the most accurate prediction of the dynamic behavior of any electronic circuit under any excitation and, in particular, it is suitable to analyze the effects of RFI on analog IC operation.

Nonetheless, this method is not efficient for RFI susceptibility analysis. In fact, when the effects of RF signals on baseband circuits are investigated, the largest sampling step in (2.5) should be much smaller than the frequency of RF signals (for a good accuracy, at least ten samples per period are required), while the overall simulation time should be much longer than the slowest time constant in the circuit, in order to reach the steady-state condition. For instance, if the effects of a 1GHz CW RF interference on a low frequency amplifier with a nominal bandwidth of 10kHz is investigated, a simulation step of less than 100ps and a simulation time of more than 500μs are required, as a consequence, more than five million samples are necessary and the simulation time can consequently be very long.

Furthermore, time-domain computer simulations do not provide a deep insight in the mechanisms which induce failures in analog IC operation: in particular, they do not relate the failures to particular circuit blocks nor they relate them to specific design parameters and parasitics. Therefore, time-domain computer simulation

cannot be employed as a primary tool in the design of analog ICs immune to EMI, although they can are valuable both for the validation of simpler models and for post-design EMI immunity test on analog sub-systems.

Piecewise Linear Approximation

An approximated solution of circuit equations (2.3) and (2.4) can be obtained in the time domain by piecewise linear approximation of function **F** in (2.4).

Employing this approach, the nonlinear system (2.4), can be written in the form

$$\begin{array}{rcll} \dot{\mathbf{x}}(t) & = & \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{e}(t) & \text{for} \quad \mathbf{x}(t),\mathbf{e}(t) \in S_1 \\ \dot{\mathbf{x}}(t) & = & \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{e}(t) & \text{for} \quad \mathbf{x}(t),\mathbf{e}(t) \in S_2 \\ & & \dots & \\ \dot{\mathbf{x}}(t) & = & \mathbf{A}_N\mathbf{x}(t) + \mathbf{B}_N\mathbf{e}(t) & \text{for} \quad \mathbf{x}(t),\mathbf{e}(t) \in S_N \end{array} \tag{2.6}$$

where $S_1 \dots S_N \in \mathbf{R}^m$ is a partition of $\mathbf{R}^m$. In each region of the state and input space the system is described by an unique set of linear differential equations. The linear ODE corresponding to the region which includes the initial condition point $\mathbf{x}(0)$,$\mathbf{e}(0)$ is firstly solved, then, if the solution reaches the border of the definition region, the linear ODE which describes the circuit in this region is solved with the border point as initial condition. This procedure is repeated until the analysis time is elapsed and/or a steady-state (limit cycle) solution is obtained.

Although piecewise linear approximation techniques provide closed-form analytical expressions of the output signals of nonlinear circuits, these techniques are not particularly suitable to the analysis of the effects of EMI in analog circuits. In fact, the nonlinear characteristics of physical electronic devices employed in analog circuits are usually smooth in their nominal region of operation therefore an accurate piecewise linear approximation would require a very fine partition, which makes the analysis of these circuits impractical. Furthermore, it is rather difficult to extract analytically from the piecewise-defined output waveforms which are obtained by this technique the parameters which are employed to quantify the effects of EMI in analog circuits (i.e. offset voltage, intermodulation products, etc...) and consequently, the relation between EMI susceptibility and circuit parameters which could be obtained would be rather involved for design purposes.

2.2.2 Frequency-Domain Steady-State Techniques

Frequency-domain analysis of analog circuits is very often much more expressive than the analysis of time-domain output waveforms. Frequency-domain analysis, in fact, is the natural tool for linear circuit analysis and highlights the most important features of electrical signals and systems. This consideration is valid, in particular, for the analysis of the effects of EMI. The concept of the influence of out-of-band disturbances in in-band circuit operation, for instance, refers to frequency domain analysis. For this reason, the techniques which provide results on the distortion of analog circuits directly in the frequency domain are particularly attractive.

Frequency-domain steady-state techniques are based on the assumption that both the input signals and the steady state output signals are periodic with the same fundamental frequency ω_0 and they can be conveniently described in terms of Fourier series expansion

$$x(t) = \sum_{n=-\infty}^{+\infty} X_n \mathrm{e}^{\mathrm{j}n\omega_0 t} \tag{2.7}$$

$$y(t) = \sum_{n=-\infty}^{+\infty} Y_n \mathrm{e}^{\mathrm{j}n\omega_0 t}. \tag{2.8}$$

This assumption makes these methods suitable to the analysis of harmonic distortion in weakly nonlinear systems while they may not be suitable to describe stronger nonlinear phenomena like chaos, in which non-periodic steady state behavior can be observed.

Rather than on the time-domain solution of the ODE (2.4), frequency domain methods are aimed to express the Fourier coefficients of the output signals Y_n in terms of the coefficients of the input signals X_n in an algebraic form. To this purpose, different techniques have been proposed in the literature, which can be suitable either for pen-and-paper or computer-aided analysis.

In the following, the Harmonic Balance, Volterra series and Describing Function methods are briefly discussed and, in particular, their suitability in RFI susceptibility design-oriented analysis is discussed.

Harmonic Balance

Harmonic Balance technique is a widely employed frequency domain analysis technique for computer-aided circuit simulation. According to Harmonic Balance technique, both the state vector $\mathbf{x}(t)$ and the excitation vectors $\mathbf{e}(t)$ are expanded in a truncated Fourier series where the first N harmonics of the fundamental frequency ω_0 are considered

$$\mathbf{x}(t) = \sum_{n=-N}^{+N} \mathbf{X}_n \mathrm{e}^{\mathrm{j}n\omega_0 t} \tag{2.9}$$

$$\mathbf{e}(t) = \sum_{n=-N}^{+N} \mathbf{E}_n \mathrm{e}^{\mathrm{j}n\omega_0 t}. \tag{2.10}$$

The above expressions of $\mathbf{e}(t)$ and $\mathbf{x}(t)$ are substituted in (2.4), which becomes

$$\sum_{n=-N}^{+N} \mathrm{j}n\omega_0 \mathbf{X}_n \mathrm{e}^{\mathrm{j}n\omega_0 t} - \mathbf{F}\left(\sum_{n=-N}^{+N} \mathbf{X}_n \mathrm{e}^{\mathrm{j}n\omega_0 t}, \sum_{n=-N}^{+N} \mathbf{E}_n \mathrm{e}^{\mathrm{j}n\omega_0 t}\right) = 0 \tag{2.11}$$

Thanks to the Fourier representation, the derivative of the state vector is computed analytically and the ODE system (2.4) reduces to an algebraic relation between time domain waveform (2.11), where the unknowns are the Fourier series coefficients X_n.

Harmonic balance technique is aimed to find out a set $\mathbf{X}$ of coefficients $\mathbf{X}_n$ in terms of the set $\mathbf{E}$ of coefficients $\mathbf{E}_n$ which satisfy, i.e. "balance", Eqn. (2.11). In general, as the solution is not exactly represented by its truncated Fourier series representation, it is not possible to find out a set of coefficients which satisfy (2.11) exactly. Nonetheless, it is possible to find out the set of coefficients which provide the best truncated Fourier series approximation of the solution. To this purpose, as Eqn. (2.11) is in the form

$$\tilde{\mathbf{F}}(\mathbf{X},\mathbf{E},t) = 0 \tag{2.12}$$

and $\tilde{\mathbf{F}}$ is periodic in time with fundamental frequency ω_0, it can be expanded in Fourier series as

$$\tilde{\mathbf{F}}(\mathbf{X},\mathbf{E},t) = \sum_{n=-\infty}^{+\infty} \tilde{\mathbf{F}}_n(\mathbf{X},\mathbf{E}) \mathrm{e}^{\mathrm{j}n\omega_0 t}. \tag{2.13}$$

Therefore, Eqn.(2.12) can be expressed in terms of the Fourier coefficients of $\tilde{\mathbf{F}}$ as

$$\tilde{\mathbf{F}}_n(\mathbf{X},\mathbf{E}) = 0 \qquad n = 0,1,\ldots,+\infty \tag{2.14}$$

which is an infinite set of complex nonlinear algebraic equations in $\mathbf{X}$ and $\mathbf{E}$. Solving the first $N+1$ equations

$$\tilde{\mathbf{F}_n}(\mathbf{X},\mathbf{E}) = 0 \qquad n = 0,1,\ldots,N \tag{2.15}$$

it is possible to obtain the $N+1$ unknown Fourier coefficients $\mathbf{X}$ of the state vector. The solution of this nonlinear algebraic system can be efficiently found by *ad hoc* numerical techniques. The details on the numerical implementation of this technique can be found in [23].

Harmonic Balance technique, which is well known in microwave circuit analysis, can be employed in EMI susceptibility analysis as a valid alternative to time-domain computer simulations [27]. Such a technique, in fact, if the number N of frequencies in the truncated Fourier expansion is sufficiently high, shows almost the same accuracy of time-domain transient simulation with a substantial improvement in terms of computational efficiency. In particular, the computational overhead of transient simulations in the analysis of circuits with very slow time constants excited by RF signals is completely avoided.

Nonetheless, Harmonic Balance is a computer simulation oriented technique like transient simulation, therefore it does not give insight in the nonlinear mechanisms which induce distortion in analog ICs nor relates RFI-induced failures to design parameters and parasitic elements. For this reason, Harmonic Balance may replace time-domain simulation in post-design EMI susceptibility investigations and in the validation of simpler analytical models but it cannot be directly employed in the design of analog ICs robust to EMI.

Volterra Series

Volterra series method is a powerful tool in the analysis of weakly nonlinear systems. This method, which was formulated by the Italian mathematician Vito Volterra in [28] in the XIX century, has been extensively employed in the analysis of weakly nonlinear electronic circuits since the beginning of the XX century [29, 30, 31].

According to Volterra series representation, in a d-input weakly nonlinear system, a generic output signal $y(t)$ can be expressed in the form

$$y(t) = \sum_{i=0}^{+\infty} y^{(i)}(t) \tag{2.16}$$

in which

$$y^{(0)} = y_0, \tag{2.17}$$

$$\begin{aligned} y^{(i)}(t) \;=\; & \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h^{k_1,\ldots,k_i}(\tau_1,\ldots,\tau_i) \\ & x_{k_1}(t-\tau_1)\ldots x_{k_i}(t-\tau_i)\,\mathrm{d}\tau_1\ldots\mathrm{d}\tau_i \end{aligned} \tag{2.18}$$

where $h^{k_1,\ldots,k_i}(\tau_1,\ldots,\tau_i)$ with $1 \le k_i \le d$ is the i-order time-domain tensor Volterra kernel, $x_{k_i}(t)$ is the time domain input tensor (for each value of the index k_i it

represents a scalar input of the system) and the product

$$p = h^{k_1,\ldots,k_i}(\tau_1,\ldots,\tau_i)\, x_{k_1}(t-\tau_1)\ldots x_{k_i}(t-\tau_i)$$

is an inner tensor product, i.e.

$$p = \sum_{k_1=1}^{d}\cdots\sum_{k_i=1}^{d} h^{k_1,\ldots,k_i}(\tau_1,\ldots,\tau_i)\, x_{k_1}(t-\tau_1)\ldots x_{k_i}(t-\tau_i)\,. \tag{2.19}$$

It is to be observed that the Volterra kernel representation in (2.16) is not unique, in fact, equivalent representations of the same system can be obtained by permutation of variables τ_k in the Volterra kernels. A unique Volterra kernel representation can be obtained if only symmetric kernels are considered, i.e. kernels which are invariant for any permutation of the variables τ_k. In the following only symmetric Volterra kernel representations will be considered.

A Volterra series model is said to be of the n-th order if the sum in (2.16) is truncated to $i = n$, i.e. if it includes only kernels up to order n. An equivalent expression for $y^{(i)}(t)$ in (2.16) can be obtained using frequency-domain Volterra kernels. In this case

$$\begin{aligned} y^{(i)}(t) \;=\; & \frac{1}{(2\pi)^i}\int_{-\infty}^{+\infty}\cdots\int_{-\infty}^{+\infty} H^{k_1,\ldots,k_i}(\omega_1,\ldots,\omega_i) \\ & X_{k_1}(\omega_1)\ldots X_{k_i}(\omega_i)\, e^{\mathrm{j}\omega_1 t}\cdots e^{\mathrm{j}\omega_i t}\mathrm{d}\omega_1\ldots\mathrm{d}\omega_i \end{aligned} \tag{2.20}$$

where $X_{k_i}(\omega)$ is the frequency domain input tensor (for each value of the index k_i it represents the Fourier transform of a system input) and the frequency domain Volterra kernels $H^{k_1,\ldots,k_i}(\omega_1,\ldots,\omega_i)$ are the i-fold Fourier transforms of the time-domain Volterra kernels and they are expressed by

$$\begin{aligned} H^{k_1,\ldots,k_i}(\omega_1,\ldots,\omega_i) \;=\; & \int_{-\infty}^{+\infty}\cdots\int_{-\infty}^{+\infty} h^{k_1,\ldots,k_i}(\tau_1,\ldots,\tau_i) \\ & e^{-\mathrm{j}\omega_1\tau_1}\cdots e^{-\mathrm{j}\omega_i\tau_2}\mathrm{d}\tau_1\ldots\mathrm{d}\tau_i. \end{aligned} \tag{2.21}$$

The product

$$H^{k_1,\ldots,k_i}(\omega_1,\ldots,\omega_i)\, X_{k_1}(\omega_1)\ldots X_{k_i}(\omega_i)$$

is an inner tensor product as before.

Finally, performing the Fourier transform of (2.16) and (2.21) one gets

$$Y(\omega) = \sum_{i=0}^{+\infty} Y^{(i)}(\omega) \tag{2.22}$$

where

$$Y^{(0)}(\omega) = y_0\delta(\omega) \tag{2.23}$$

and

$$\begin{aligned} Y^{(i)}(\omega) \;=\; & \int_{-\infty}^{+\infty}\cdots\int_{-\infty}^{+\infty} H^{k_1,\ldots,k_i}\left(\omega_1,\ldots,\omega-\sum_{n=1}^{i-1}\omega_n\right) \\ & X_{k_1}(\omega_1)\ldots X_{k_i}\left(\omega-\sum_{n=1}^{i-1}\omega_n\right)\mathrm{d}\omega_1\ldots\mathrm{d}\omega_{i-1} \end{aligned} \tag{2.24}$$

Equation (2.22) relates the spectrum of the output signals to the spectra of the input signals and justifies the classification of Volterra series method among frequency domain analysis methods.

Volterra series can be considered either as the generalization of Taylor series analysis, which is suitable to describe nonlinear memoryless systems, or as the generalization of frequency-domain analysis, which is suitable to describe linear dynamic systems, in order to describe the behavior of (weakly) nonlinear dynamic systems.

In fact, it can be observed that in the case of a memoryless system, i.e. a system in which the output signals depend only on the present value of the input signals, the Volterra kernels can be written as

$$h^{k_1,\ldots,k_i}(\tau_1,\ldots,\tau_i) = \hat{h}^{k_1,\ldots,k_i}\delta(\tau_1)\delta(\tau_2)\cdots\delta(\tau_i),$$

where $\hat{h}^{k_1,\ldots,k_i}$ is a scalar constant independent of τ_i, therefore, from (2.19),

$$y^{(i)}(t) = \hat{h}^{k_1,\ldots,k_i}x_{k_1}(t)x_{k_2}(t)\ldots x_{k_i}(t) \tag{2.25}$$

and (2.16) reduces to the Taylor series expansion of the output signal of a d-input nonlinear memoryless system.

It can be also observed from (2.16) that first-order Volterra kernels $h^{k_1}(\tau_1)$, i.e. the kernels for which $i = 1$, are the linear system pulse responses for an input excitation $\delta(t-\tau_1)$ applied as the k_1-th system input and consequently, the first-order frequency domain kernels $H^{k_1}(\omega_1)$ are the linear frequency domain transfer functions.

Volterra series method is particularly attractive in the analysis of harmonic distortion and, in particular, for the prediction of the susceptibility to RFI of analog integrated circuits. In fact Volterra series allow a closed-form calculation of the RFI-induced harmonic components in the spectra of analog circuit output signals in terms of design parameters and parasitic elements. This feature makes Volterra analysis very useful in the design of analog integrated circuits robust to EMI.

Nonetheless, Volterra series method suffers of some limitations: in particular, this method is particularly suitable to the description of weakly nonlinear systems with

polynomial nonlinearity, while non-polynomial nonlinearity can only be described through high order Volterra models which can be very complex. In particular, a nonlinear characteristic which is not continuous and smooth (i.e. derivable up to high orders) in a given interval cannot be properly represented by Volterra series expansion of any order. Therefore, with reference to the analysis of electronic circuits, Volterra series can accurately predict the nonlinear polynomial behavior of MOS (BJT) devices biased in their saturation (active) region of operation while they can describe very poorly their threshold (switching) characteristics.

On the basis of these considerations, unlike computer simulation techniques, Volterra series analysis is very accurate only as far as the amplitude of the input signal and/or disturbances keeps the active devices within their nominal region of operation, while it is no longer reliable when the amplitude of RFI excites the threshold effect in the nonlinear characteristics.

Volterra series method will be employed in the following Chapter for the derivation of a model for the prediction of the susceptibility of integrated opamp circuits to RFI superimposed onto the nominal input signals and/or onto the power supply rails.

Describing Function

Describing function method can be considered as a simplified version of the Harmonic Balance technique which is suitable to closed-form calculations. This method, in particular, is effective for the frequency-domain analysis of weakly nonlinear dynamical systems which include only one insulated memoryless nonlinearity.

According with the describing function method, a memoryless nonlinearity $f(x)$ is described in the frequency domain in terms of the harmonic content of its output signal when its input is a harmonic signal

$$x(t) = A\cos(\omega t + \varphi).$$

In this case, the output signal

$$y(t) = f(x(t)) = f(A\cos(\omega t + \varphi))$$

is a periodic signal with fundamental frequency ω, therefore it can be expanded in Fourier series as

$$y(t) = \sum_{n=0}^{+\infty} H_n(A,\omega,\varphi)\cos(\omega t + \varphi_H(A,\omega,\varphi)) \tag{2.26}$$

The Fourier expansion coefficients $H_n(A,\omega,\varphi)$ and $\varphi_H(A,\omega,\varphi)$ describe the operation of the nonlinear system in terms of the parameters (amplitude, frequency and

phase) of the input harmonic signal therefore they are referred to as *describing functions*. In other words, the describing function method characterizes the harmonic response of nonlinear systems in terms of amplitude and phase dependent frequency domain transfer functions. A describing function analysis of a nonlinear dynamical systems can be obtained on the bases of the frequency-domain characterization of the memoryless nonlinear section of the system and on the transfer functions which describe the linear section.

This method, which is widely employed in control theory, can be also employed in the analysis of the susceptibility of analog ICs to EMI. To this purpose, the describing function method is particularly attractive as it does not suffer of the limitation in terms of signal amplitude of Volterra series method and lets to relate the susceptibility to EMI of analog circuits to design parameters and parasitics. Nonetheless, unlike Volterra series method, its application is not straightforward and systematic. Analog circuits, in facts, typically include much more than a single memoryless nonlinearity and, furthermore, the signals which feed the nonlinearity are not pure harmonic signals. For these reasons, the main nonlinear mechanisms which are responsible of the EMI-induced failures in analog circuits should be firstly highlighted and *ad hoc* simplified models of the analog circuits should be developed which focus the main nonlinear effects. If the describing function method is properly employed, very accurate and effective analytical models for the prediction of the susceptibility to EMI of analog circuits may be derived.

Chapter 3

Prediction of Operational Amplifier Susceptibility to RFI

Integrated operational amplifiers (opamps), which are probably the most common and versatile analog building blocks in analog circuit design, have proven to be very susceptible to RFI superimposed onto their input terminals and/or onto the power supply rails. The susceptibility to RFI of IC opamp deserves a particular attention not only for the widespread diffusion of opamp circuits in more complex analog sub-systems but also because the case of opamp circuits is emblematic of the main aspects which should be taken into account in the prediction of the susceptibility to RFI of analog ICs.

In this Chapter the susceptibility to EMI of integrated operational amplifiers is investigated. To this purpose, three different analytical models which predict the behavior of integrated opamp circuits in the presence of RFI are presented. After some basic considerations on the structure of integrated opamp circuits, the susceptibility of opamp ICs subjected to RFI superimposed onto the input voltages is investigated through Volterra series analysis. Then, Volterra series analysis is extended in order to take into account the demodulation of RFI superimposed onto opamp power supply rails.

Furthermore, the numerical model which has been proposed by Fiori in [20] for the prediction of the RFI-induced offset voltage in opamp circuits under large-signal excitation has been reconsidered. In particular, this model has been extended in order to provide a closed-form expression of the RFI-induced offset voltage in opamp circuits and in order to highlight the dependence on RFI frequency of the RFI-induced offset has been highlighted. This extension overcomes the limit of Volterra series analysis in closed-form prediction of the distortion induced by large signal RFI in opamp circuits.

All the models which are discussed in this Chapter are validated by comparison

of model predictions and direct injection on-wafer CW RFI susceptibility measurements which have been carried out on opamp test chips that have been designed and diffused on silicon to this purpose.

3.1 Nonlinear Effects of RF Interference in Opamps

In this Section some qualitative considerations on the main nonlinear phenomena which may induce RFI distortion within IC opamp circuits are discussed. In particular, RF and baseband signal propagation within an opamp circuit is firstly investigated, then the peculiar role in RFI susceptibility which is played by the opamp input stage is highlighted and a general-purpose opamp macromodel for RFI susceptibility investigation is presented. Finally, more insight on the relation between the differential pair RFI-induced distortion and its parasitic capacitances is provided.

On the bases of these considerations, reported in [32, 33], the models which are presented in the following will be derived.

3.1.1 Signal Propagation within Operational Amplifiers

Previous work shown that the nonlinear mechanisms that cause the demodulation of RFI which is superimposed onto the input terminals of CMOS opamps are almost only due to the input differential pair [12, 15]. This fact, that has also been experimentally verified, can be ascribed to two concurrent causes which are related to the propagation of RFI and baseband signals throughout CMOS opamps.

In particular, in order to evaluate in-band distortion of out-of-band RFI, an opamp can be regarded as the cascade connection of elementary amplifying stages, the first of which is usually a differential pair (Fig. 3.1). Each amplifying stage shows an amplification $A_i(\omega)$ which is very high within its nominal bandwidth $\omega_{\mathrm{B},i}$ while it is very low (about zero) out of this bandwidth, i.e.

$$\begin{cases} |A_i(\omega)| \gg 1 & \text{for} \quad \omega < \omega_{\mathrm{B},i} \\ |A_i(\omega)| \simeq 0 & \text{for} \quad \omega > \omega_{\mathrm{B},i}. \end{cases} \tag{3.1}$$

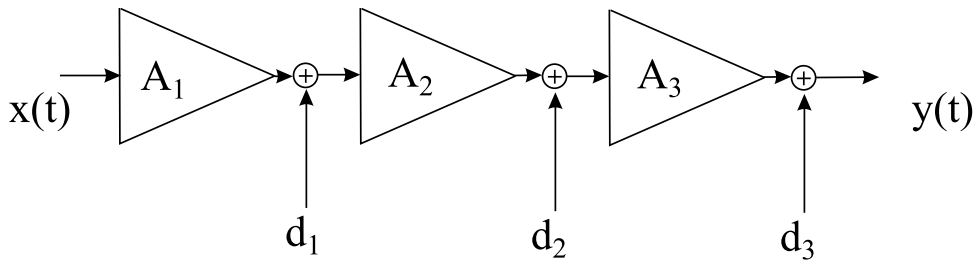


Figure 3.1. Block diagram of a three-stage amplifier.

Furthermore, each amplifying stage generates a certain amount of in-band distortion d_i due to the effects of RFI, which is related to the peak amplitude of RFI superimposed onto its input signal.

On the basis of (3.1), the out-of-band RFI that is superimposed onto the input voltages of a CMOS opamp essentially does not propagate beyond the input differential pair. In fact, if the frequency of RFI is out of the bandwidth of the differential pair, it is strongly attenuated by its transfer function. As a consequence, RFI does not reach the following stages and the amount of in-band distortion d_i, $i > 1$ which is generated by any amplifying stage which follow the differential pair, independently of its nonlinear characteristics, is intrinsically much smaller than the in-band distortion d_1 generated by the differential pair.

Furthermore, assuming for the sake of simplicity that the in-band amplification of each stage is frequency independent (i.e. $A_i\omega = A_i$), the output signal y of a three-stage opamp can be written in the form

$$\begin{aligned} y &= A_1A_2A_3x + A_2A_3d_1 + A_3d_2 + d_3 \\ &= y_{\text{nom}} + y_{\text{d}} \end{aligned} \tag{3.2}$$

in which

$$y_{\text{nom}} = A_1A_2A_3x$$

is the nominal output signal and

$$y_{\text{d}} = A_2A_3d_1 + A_3d_2 + d_3 \tag{3.3}$$

is the RFI-induced distortion.

From (3.3), the contribution of each single stage to the overall output distortion is given by the distortion generated by the stage multiplied by the amplifications of the stages that follow it. From (3.1) the in-band amplification of the cascaded stages is usually (very) high, therefore, even assuming the terms d_i of the same order of magnitude, the overall output offset is dominated by the contribution of the first stage.

From the above considerations on signal propagation within opamp circuits, it is essential to highlight the distortion phenomena induced by RFI in the input differential pair to the purpose of modelling the in-band effects of out-of-band RF interference, while the following amplifying stages can be assumed to be linear without appreciable loss of accuracy.

3.1.2 An RFI-Oriented Opamp Circuit Model

The considerations on opamp structure and signal propagations which have been presented above lead to the CMOS opamp circuit model shown in Fig.3.2. Such a circuit is composed by a differential pair cascaded with an ideal transimpedance amplifier (Z_s).

The input differential stage is made up of two source coupled nMOS transistors (M1 and M2) biased by the current source i_S and the input voltages v^- and v^+. The nonlinear characteristics of the input devices M1 and M2 are taken into account and the differential pair parasitics are properly extracted. The output signal is the current i_D, which is defined as

$$i_\mathrm{D} = i_\mathrm{D1} - i_\mathrm{D2}. \tag{3.4}$$

This current drives the linear transimpedance amplifier ($Z_\mathrm{s}(\omega)$). The transimpedance $Z_\mathrm{s}(\omega)$ is related to the open-loop differential amplification $A_\mathrm{d}(\omega)$ of the overall opamp circuit, in particular, it is given by

$$Z_\mathrm{s}(\omega) = \frac{A_\mathrm{d}(\omega)}{g_\mathrm{m}},$$

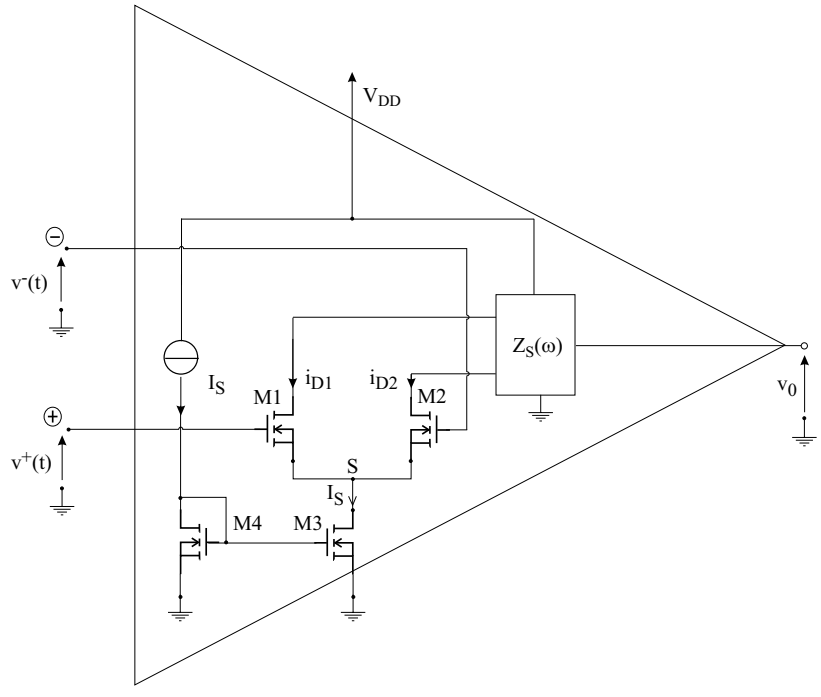


Figure 3.2. RFI-oriented opamp model.

where g_{m} is the small-signal differential transconductance of the differential pair. The input voltages v^- and v^+ in Fig.3.2 describe both nominal and interfering signals and they can be also expressed in terms of the common mode voltage

$$v_{\mathrm{CM}} = \frac{v^+ + v^-}{2}, \tag{3.5}$$

and of the differential mode voltage

$$v_{\mathrm{D}} = v^+ - v^-. \tag{3.6}$$

Such an opamp macromodel will be referred to in the following for the derivation of analytical models of the behavior of opamp circuits in the presence of EMI. To this purpose, in particular, the RFI-induced distortion in the differential pair which is included in it will be investigated.

3.1.3 Differential Pair Nonlinear Operation

Differential pairs, because of their intrinsic symmetry, are usually considered to be free from even-order distortion, which is the main cause of RFI demodulation. Nonetheless, a particular high-frequency distortion phenomenon which is related to differential pair parasitics and occurs even in perfectly matched differential pairs has been highlighted [32, 33].

This phenomenon, which is the main cause of the susceptibility of CMOS opamps to RFI, is now illustrated with reference to the differential pair circuit in Fig.3.3. Under the assumption that transistors M1 and M2 are perfectly matched and at the same temperature, the relationship between the input differential voltage v_{D} and the output differential current i_{D} is given by

$$i_{\mathrm{D}} = \begin{cases} -i_{\mathrm{S}} & v_{\mathrm{D}} \leq -\sqrt{\frac{i_{\mathrm{S}}}{\beta}} \\ v_{\mathrm{D}}\sqrt{2\beta i_{\mathrm{S}}}\sqrt{1-\frac{\beta v_{\mathrm{D}}^2}{2i_{\mathrm{S}}}} & |v_{\mathrm{D}}| \leq \sqrt{\frac{i_{\mathrm{S}}}{\beta}} \\ i_{\mathrm{S}} & v_{\mathrm{D}} \geq \sqrt{\frac{i_{\mathrm{S}}}{\beta}} \end{cases} \tag{3.7}$$

where i_{S} is the bias current of the differential pair and

$$\beta = \frac{\mu C_{\mathrm{ox}}}{2}\frac{W}{L}$$

where μ is the mobility of electrons (holes) in nMOS (pMOS) devices, C_{ox} is the capacitance of the gate oxide per unit of area and W and L are the width and the length of the gate area of the MOS devices of the pair.

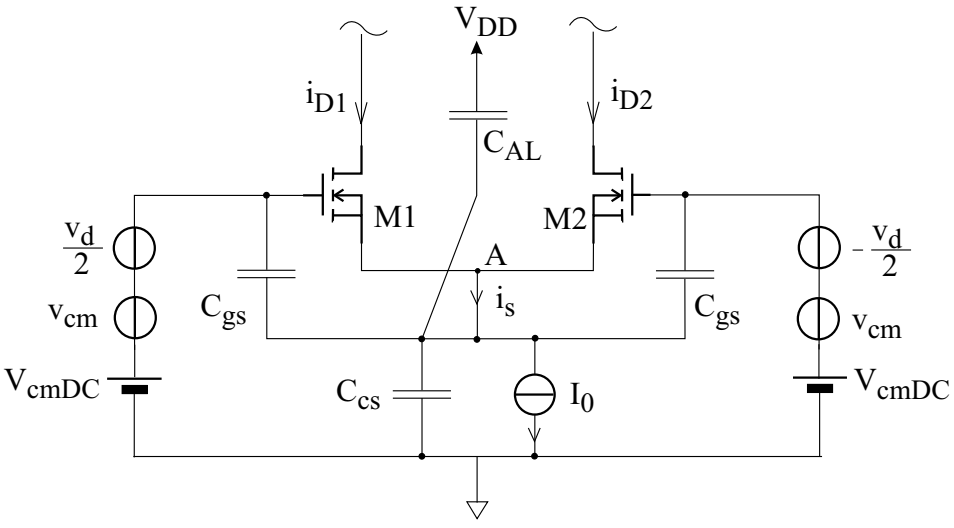


Figure 3.3. MOS Differential Pair.

Expression (3.7) is usually regarded as a function of the only variable v_{D}, while β and $i_{\mathrm{S}}(t) = I_0$ are assumed to be constant design parameters. On the basis of this assumption, a differential pair is a completely symmetrical structure and therefore it does not generates even order distortion [30]. This fact is also implicit in (3.7), which shows that the differential current i_{D} is an odd function of v_{D}. In actual differential pairs, however, because of the finite admittance of the bias current source, RF fluctuations of the input common-mode voltage cause RF fluctuations on the effective bias current i_{S} which induce even-order distortion in the differential current because of a mixing effect.

This effect can be qualitatively illustrated performing a two-input, second-order Taylor series expansion of (3.7). By so doing, the differential current i_{D} is expressed as

$$i_{\mathrm{d}} = g_{\mathrm{m}} v_{\mathrm{d}} + g_{\mathrm{p}} v_{\mathrm{d}} i_{\mathrm{s}}. \tag{3.8}$$

where

$$g_{\mathrm{m}} = \sqrt{2\beta I_0}$$

is the linear transconductance of the differential pair and

$$g_{\mathrm{p}} = \sqrt{\frac{\beta}{2I_0}}.$$

Furthermore, with reference to the differential pair shown in Fig.3.3, whose small-signal equivalent circuit is shown in Fig.3.4, the RFI fluctuations of the effective bias current can be expressed as

$$\begin{aligned} I_{\mathrm{s}}(\mathrm{j}\omega) &= V_{\mathrm{cm}}(\mathrm{j}\omega)\,\frac{2g_{\mathrm{m}}\mathrm{j}\omega C_{\mathrm{T}}}{\mathrm{j}\omega\,(2C_{\mathrm{gs}} + C_{\mathrm{T}}) + 2g_{\mathrm{m}}} \\ &= V_{\mathrm{cm}}(\mathrm{j}\omega)\,Y(\mathrm{j}\omega). \end{aligned} \tag{3.9}$$

where

$$C_{\mathrm{T}} = C_{\mathrm{cs}} + C_{\mathrm{AL}}$$

is the parasitic capacitance connected between node S and AC ground whereas $V_{\mathrm{d}}(\mathrm{j}\omega)$ and $V_{\mathrm{cm}}(\mathrm{j}\omega)$ are respectively the differential and the common mode component of the input voltage in the frequency domain, as shown in Fig.3.4.

Eqn.(3.8) shows that, in the presence of RF fluctuations of the bias current, a differential pair acts as a mixer and performs the product between the RF components of v_{D} and i_{S}. Furthermore, because of the parasitic capacitance C_{T}, as shown in (3.9), RF interference superimposed onto opamp input terminals induces RF fluctuations on the input differential voltage and on the bias current. As a consequence, the above mentioned mixing effect results in second-order distortion and in RFI demodulation.

On the basis of such considerations, the parasitic capacitances of the input differential pair strongly influence the susceptibility to EMI of CMOS opamps, for this reason the next Section is devoted to the physical origin of these parasitic capacitances.

3.1.4 Physical Origin of Differential Pair Parasitics

The parasitic capacitances which are included in a differential pair play a fundamental role in the susceptibility to RFI of CMOS opamps, as it has been highlighted in the previous Section, therefore it is meaningful to trace each parasitic capacitance back to its physical origin on the basis of the cross section of a CMOS technology process shown in Fig.3.5.

With reference to the nMOS differential pair in Fig.3.6a and to the cross section of an nMOS transistor in a standard twin-tub CMOS process which is provided in Fig.3.5a, C_{db3} represents the drain-body reverse junction capacitance of transistor M3 while C_{gs1} and C_{gs2} in Fig.3.6a are the gate-to-source capacitances of transistors M1 and M2 respectively. The capacitance C_{AL} in the same figure is related to the reverse biased junction between p-well and n-isolation as shown in Fig.3.5a. The parasitic capacitance C_{sb} of M1 and M2 is not relevant because it is shorted by the connection between body and source.

If the p-well in which the differential pair is laid out is tied to ground, or if a single-well bulk CMOS process is employed and nMOS transistors are laid out directly on the substrate, as shown in Fig.3.7, the parasitic capacitance C_{AL} is either connected between power supply and ground or it is absent at all. In both cases, it

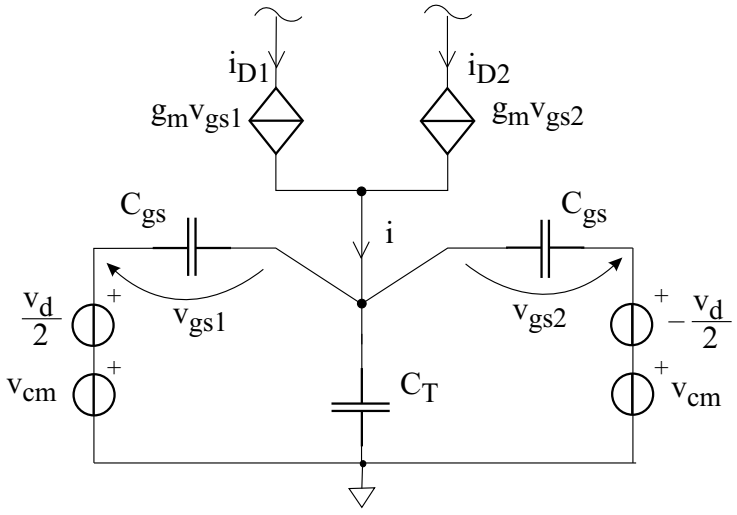


Figure 3.4. Small signal equivalent circuit of the differential pair.

is not included in the signal path. In this case, however, the parasitic capacitances C_{sb} of the input devices is connected between the common source node and ground and plays the same role in of C_{AL} in the distortion of RFI.

With reference to Fig.3.6b and Fig.3.5b, the origin of the parasitic capacitances in a pMOS differential pair can be traced back in a similar way. It has to be noted that, in this case, the role of C_{AL} is played by C_{GND}, i.e. the capacitance of the reverse biased junction between n-well and the substrate. If the differential pair n-well is connected to the power supply voltage, C_{GND} is no longer relevant and its role is played by C_{sb}.

From the above analysis it can be pointed out that the parasitic capacitances C_{AL} and C_{GND} or C_{sb}, which are included in the parasitic capacitance C_{T} in (3.9), both depends on the layout of the differential pair. Therefore, an accurate prediction of this capacitance and, consequently, of the susceptibility of a given differential pair to EMI, can be made only on the basis of the physical layout of the circuit. Furthermore, the results on the effects of differential pair parasitics on the susceptibility to EMI can be translated into layout rules to increase the immunity to EMI.

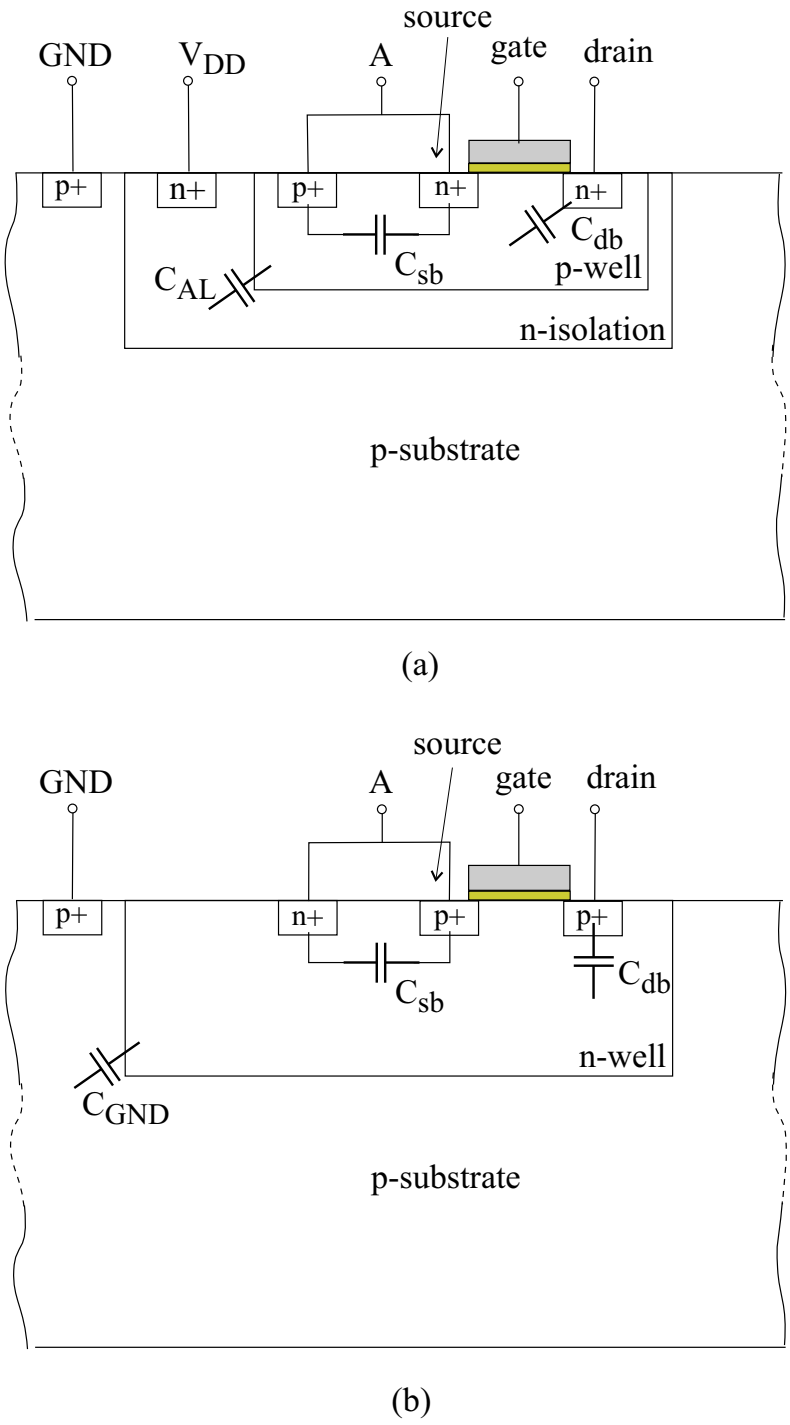


Figure 3.5. Cross section of a twin-tub CMOS technology process.

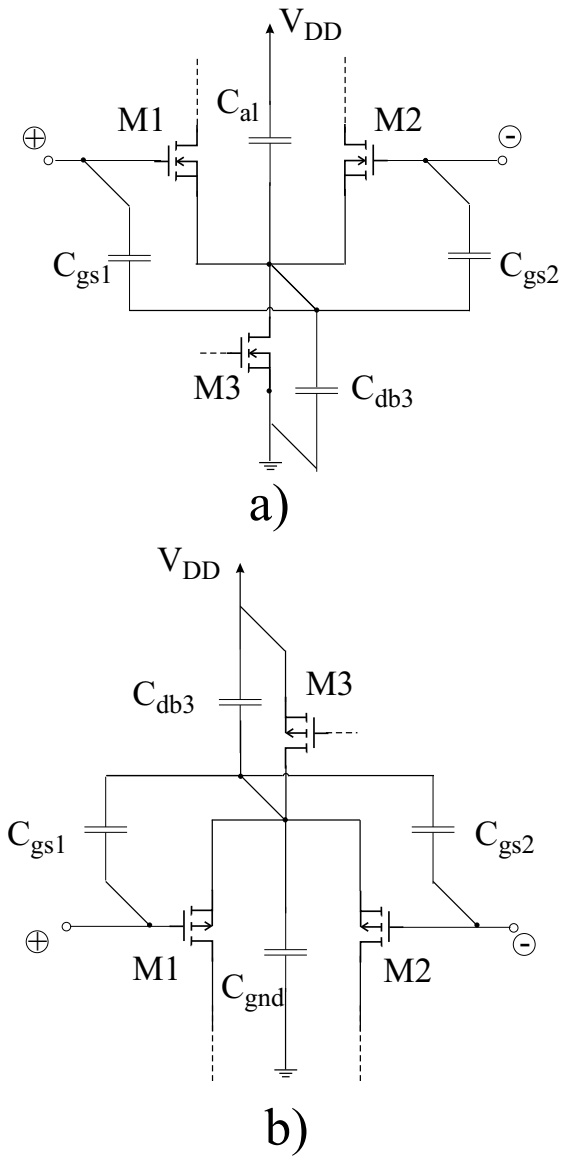


Figure 3.6. Insulated-well differential pair parasitic capacitances.

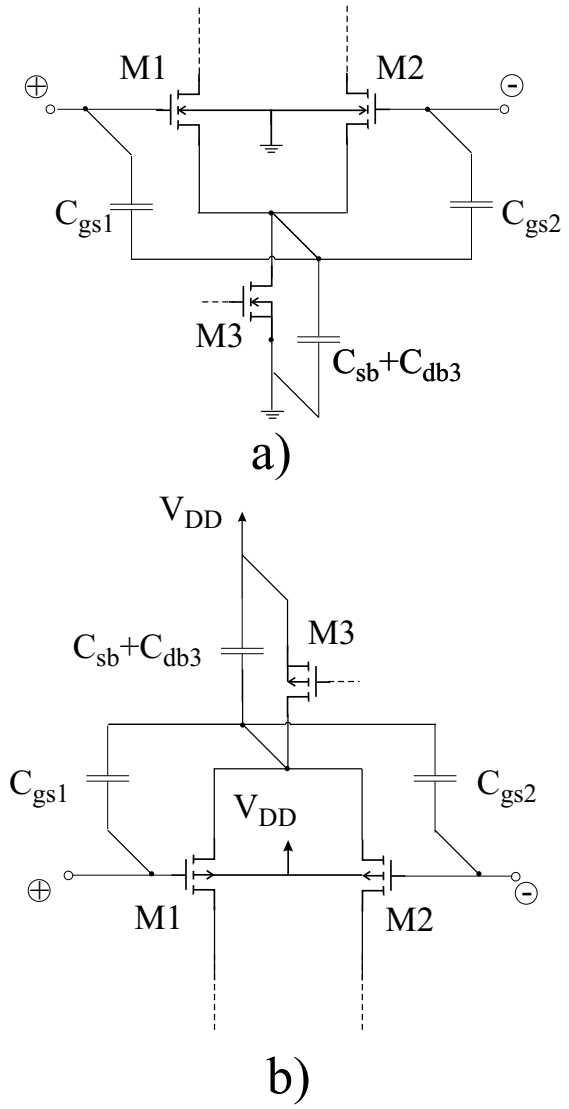


Figure 3.7. Bulk differential pair parasitic capacitances.

3.2 A Two-Input Volterra Series Opamp Model

Volterra series are a very powerful analytical tool to describe nonlinear effects in weakly nonlinear dynamic systems. This analytical method, which has been already described in Section 2.2.2, provides the natural extension of frequency domain analysis to nonlinear systems and it enables to relate the nonlinear distortion properties of circuits to design parameters and to parasitics. These features make this approach particularly attractive in the modelling of the nonlinear effects of RFI in operational amplifiers.

Even though Volterra series have been extensively employed to predict harmonic distortion in analog integrated circuits and, in particular, in opamp circuits, the models which have been previously developed [30] were focused to in-band distortion and, in particular, do not include the high frequency distortion effect due to the differential pair parasitic capacitances which has been highlighted in the previous Section. Therefore, these models are not suitable to the prediction of the effects of RFI in opamp operations.

In this Section a new Volterra series model which is suitable to predict the distortion phenomena which are induced by RFI superimposed onto the input terminals in the generic opamp circuit shown in Fig.3.8 is presented. In particular, it will be shown that a two-input Volterra series model is required to this purpose. To this purpose, with reference to the Volterra series notation which has been introduced in Section 2.2.2, a two-input second-order Volterra model will be derived and it will be employed to predict the RFI-induced DC offset voltage in feedback opamp circuits. Finally, model prediction will be compared with the results of on-wafer susceptibility measurements which have been carried out on opamp test chips that have been designed and diffused on silicon to this purpose. The results of this analysis have been published in [34].

3.2.1 Two-Input Volterra Series Model Derivation

In order to predict the nonlinear effects induced by RFI superimposed onto the input terminals V^+ and V^- in the arbitrary opamp circuit shown in Fig.3.8, a two-input, second-order Volterra series model is derived.

A two input model is necessary in order to take into account the high frequency distortion phenomena discussed in Section 3.1.3, while a series expansion up to the second order is sufficient for an accurate analysis of the effect of RFI. In fact, it has been observed that third-order distortion does not translate out-of-band RFI into in-band interference and the fourth-order and higher-order terms only give minimal contributions to the overall demodulation of RFI, which do not justify a substantial increase in model complexity. In particular, the inclusion of high-order terms would not substantially improve the large-signal accuracy of a Volterra

series model because the threshold characteristics of MOS transistors can not be conveniently approximated by a polynomial function.

In the following, a Two-Input, Second-Order Volterra series model of the opamp input differential pair is firstly derived. Such a model, in particular, takes into account the high-frequency nonlinear effects which have been highlighted in Section 3.1.3. From this differential pair model, the model of an open loop operational amplifier on the basis of the opamp circuit for EMI analysis shown in Fig.3.2 is obtained. Finally, the Volterra kernel description of the general, linear negative-feedback, opamp circuit shown in Fig.3.8 is presented.

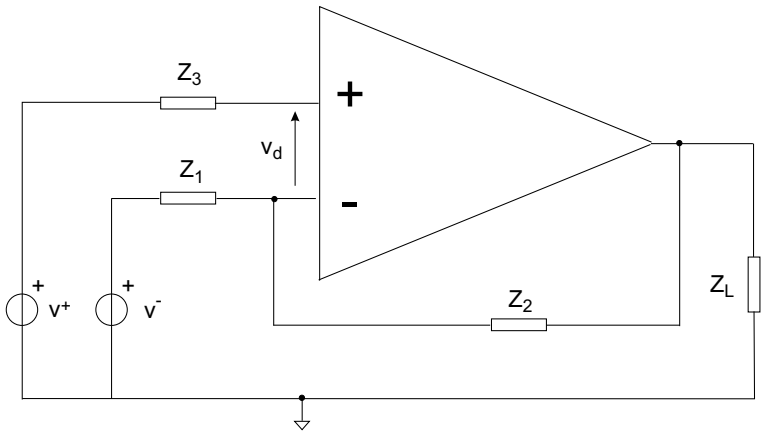


Figure 3.8. General negative feedback opamp configuration.

Differential Pair Model

A Volterra kernel description of the nonlinear operation of the differential pair, considering the differential voltage v_{D} and the effective bias current i_{S} as inputs, is directly derived from (3.10) through a Taylor series expansion in the DC bias point $(v_{\mathrm{D}},i_{\mathrm{S}}) = (0,I_0)$ and using the direct expansion method [29].

In particular, with the Volterra series tensor notation presented in Section 2.2.2, assuming the time domain input tensor $x_k(t)$ in the form

$$\begin{aligned} x_1(t) &= v_{\mathrm{d}}(t) \\ x_2(t) &= i_{\mathrm{s}}(t), \end{aligned}$$

from the nonlinear static expression which relates i_{D} to v_{D} and i_{s}

$$i_{\mathrm{D}} = \begin{cases} -i_{\mathrm{S}} & v_{\mathrm{D}} \leq -\sqrt{\frac{i_{\mathrm{S}}}{\beta}} \\ v_{\mathrm{D}}\sqrt{2\beta i_{\mathrm{S}}}\sqrt{1-\frac{\beta v_{\mathrm{D}}^2}{2i_{\mathrm{S}}}} & |v_{\mathrm{D}}| \leq \sqrt{\frac{i_{\mathrm{S}}}{\beta}} \\ i_{\mathrm{S}} & v_{\mathrm{D}} \geq \sqrt{\frac{i_{\mathrm{S}}}{\beta}} \end{cases} \tag{3.10}$$

the symmetric time-domain Volterra kernels can be derived by Taylor series expansion

$$\begin{aligned} i_{\mathrm{D}}^{(2)} = i_{\mathrm{D}}|_{0,I_0} &+ \left.\frac{\partial i_{\mathrm{D}}}{\partial v_{\mathrm{D}}}\right|_{0,I_0} v_{\mathrm{d}} + \left.\frac{\partial i_{\mathrm{D}}}{\partial i_{\mathrm{S}}}\right|_{0,I_0} i_{\mathrm{s}} + \\ &+ \frac{1}{2}\left.\frac{\partial^2 i_{\mathrm{D}}}{\partial v_{\mathrm{D}}^2}\right|_{0,I_0} v_{\mathrm{d}}^2 + \frac{1}{2}\left.\frac{\partial^2 i_{\mathrm{D}}}{\partial i_{\mathrm{S}}^2}\right|_{0,I_0} i_{\mathrm{s}}^2 + \left.\frac{\partial^2 i_{\mathrm{D}}}{\partial v_{\mathrm{D}}\partial i_{\mathrm{S}}}\right|_{0,I_0} v_{\mathrm{d}} i_{\mathrm{s}} \end{aligned} \tag{3.11}$$

where

$$\begin{aligned} i_{\mathrm{D}}|_{0,I_0} &= 0 \\ \left.\frac{\partial i_{\mathrm{D}}}{\partial v_{\mathrm{D}}}\right|_{0,I_0} &= g_{\mathrm{m}} = \sqrt{2\beta I_0} \\ \left.\frac{\partial i_{\mathrm{D}}}{\partial i_{\mathrm{S}}}\right|_{0,I_0} &= \frac{1}{2}\left.\frac{\partial^2 i_{\mathrm{D}}}{\partial v_{\mathrm{D}}^2}\right|_{0,I_0} = \frac{1}{2}\left.\frac{\partial^2 i_{\mathrm{D}}}{\partial i_{\mathrm{S}}^2}\right|_{0,I_0} = 0 \\ \left.\frac{\partial^2 i_{\mathrm{D}}}{\partial v_{\mathrm{D}}\partial i_{\mathrm{S}}}\right|_{0,I_0} &= \sqrt{\frac{\beta}{2I_0}}. \end{aligned} \tag{3.12}$$

On the basis of the Taylor series coefficients, the time-domain Volterra kernels can be derived by the direct expansion method [29] and take the form

$$h^1(\tau_1) = \sqrt{2\beta I_0}\delta(\tau_1) = g_{\mathrm{m}}\delta(\tau_1)$$

$$h^2(\tau_1) = 0$$

$$h^{11}(\tau_1,\tau_2) = 0 \qquad h^{12}(\tau_1,\tau_2) = \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\delta(\tau_1)\delta(\tau_2)$$
$$h^{21}(\tau_1,\tau_2) = \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\delta(\tau_1)\delta(\tau_2) \quad h^{22}(\tau_1,\tau_2) = 0.$$

Consequently, from (2.22) the frequency domain Volterra kernels can be computed. In particular, considering the input tensor

$$\begin{aligned} X_1(\omega) &= V_{\mathrm{d}}(\omega) \\ X_2(\omega) &= I_{\mathrm{s}}(\omega) \end{aligned} \tag{3.13}$$

and the differential pair output current $I_{\mathrm{d}}(\omega)$ [1] as the system output $Y(\omega)$, the frequency-domain Volterra kernels up to the second order are expressed in the form

$$H^1(\omega_1) = \sqrt{2\beta I_0}$$
$$H^2(\omega_1) = 0$$

$$H^{11}(\omega_1,\omega_2) = 0 \qquad H^{12}(\omega_1,\omega_2) = \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}$$
$$H^{21}(\omega_1,\omega_2) = \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}} \quad H^{22}(\omega_1,\omega_2) = 0.$$

The above Volterra kernels refer to the input tensor (3.13). This tensor includes the differential pair bias current I_{s}, which is not an external input of the differential pair. Therefore, those kernels have to be expressed in terms of the input tensor

$$\begin{aligned} X_1(\omega) &= V_{\mathrm{d}}(\omega) \\ X_2(\omega) &= V_{\mathrm{cm}}(\omega) \end{aligned} \tag{3.14}$$

which includes the differential pair input signals.

Such a result can be obtained from the first order expansion of v_{D} and i_{S} by the direct expansion method [29]. In particular, it can be observed that such a first order expansion is sufficient to obtain an *exact* second-order expansion for the differential current. If higher order terms in the expansions of v_{D} and i_{S} would have been included, such terms would generate contributions of order higher than the second and could be dropped in order to get a second-order expansion.

The first order Volterra expansion of i_{S} is obtained from the frequency domain analysis of the circuit that is shown in Fig. 3.4, which is the small signal equivalent circuit of the input differential pair. From this analysis I_{s} can be expressed in terms of the common-mode input voltage V_{cm} as

$$I_{\mathrm{s}}(\mathrm{j}\omega) = V_{\mathrm{cm}}(\mathrm{j}\omega)\,\frac{2g_{\mathrm{m}}\mathrm{j}\omega C_{\mathrm{T}}}{\mathrm{j}\omega\,(2C_{\mathrm{gs}} + C_{\mathrm{T}}) + 2g_{\mathrm{m}}} \tag{3.15}$$

[1] the small letter subscript indicates the fluctuation of the quantity indicated by the capitalized subscript around the DC quiescent bias point.

where $C_{\rm gs}$ is the gate-to-source capacitance of each transistor of the pair while $C_{\rm T}$ is the parasitic capacitance between the common source node and AC ground, whose physical origin has been discussed in Section 3.1.4.

Hence, the differential pair frequency domain Volterra kernels are given by

$$\begin{aligned} H^1(\omega_1) &= \sqrt{2\beta I_0} = g_{\rm m} \\ H^2(\omega_1) &= 0 \end{aligned}$$

$$\begin{aligned} H^{11}(\omega_1,\omega_2) &= 0 \\ H^{12}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\,\tfrac{2g_{\rm m}{\rm j}\omega_2 C_{\rm T}}{{\rm j}\omega_2(2C_{\rm gs}+C_{\rm T})+2g_{\rm m}} \\ H^{21}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\,\tfrac{2g_{\rm m}{\rm j}\omega_1 C_{\rm T}}{{\rm j}\omega_1(2C_{\rm gs}+C_{\rm T})+2g_{\rm m}} \\ H^{22}(\omega_1,\omega_2) &= 0. \end{aligned}$$

Open Loop Opamp Model

The Volterra kernel of the complete opamp circuit in Fig.3.2 can be derived by cascading the two-input Volterra system, which describes the differential pair and the linear system which describes the following stages. The linear stages which follow the differential pair are described as an amplifying block with transimpedance

$$Z_{\rm s}({\rm j}\omega) = \frac{A_{\rm d}(\omega)}{g_{\rm m}} = \frac{A_{\rm d}(\omega)}{\sqrt{2\beta I_0}}$$

where $A_{\rm d}({\rm j}\omega)$ is the differential amplification of the overall opamp.

From the cascading theorem [30] for frequency domain Volterra series and considering $X_k(\omega)$ the frequency domain input tensor

$$\begin{aligned} X_1(\omega) &= V_{\rm d}(\omega) \\ X_2(\omega) &= V_{\rm cm}(\omega), \end{aligned} \tag{3.16}$$

and the opamp output voltage $V_{\rm out}$ as the system output $Y(\omega)$, the Volterra representation of the overall opamp is the obtained

$$\begin{aligned} H^1(\omega_1) &= A_{\rm d}(\omega_1) \\ H^2(\omega_1) &= 0 \end{aligned}$$

$$\begin{aligned} H^{11}(\omega_1,\omega_2) &= 0 \\ H^{12}(\omega_1,\omega_2) &= \tfrac{1}{2}\,\tfrac{A_{\rm d}(\omega_1+\omega_2)}{2I_0}\,\tfrac{2g_{\rm m}{\rm j}\omega_2 C_{\rm T}}{{\rm j}\omega_2(2C_{\rm gs}+C_{\rm T})+2g_{\rm m}} \\ H^{21}(\omega_1,\omega_2) &= \tfrac{1}{2}\,\tfrac{A_{\rm d}(\omega_1+\omega_2)}{2I_0}\,\tfrac{2g_{\rm m}{\rm j}\omega_1 C_{\rm T}}{{\rm j}\omega_1(2C_{\rm gs}+C_{\rm T})+2g_{\rm m}} \\ H^{22}(\omega_1,\omega_2) &= 0. \end{aligned}$$

These Volterra kernels provide a complete description of an opamp and can be employed in the evaluation of distortion phenomena induced by RFI.

Negative-Feedback Opamp Circuit Model

The description of negative-feedback opamp circuits in terms of Volterra kernels is derived from the Volterra kernels opamp description presented above. To this purpose, the input voltages $V_{\rm d}(\omega)$ and $V_{\rm cm}(\omega)$ should be expressed as a function of the overall circuit input signals $V^+(\omega)$ and $V^-(\omega)$ (see Fig.3.8) and the effects of the feedback should be taken into account. The second order expansion of the output voltage ($V_{\rm out}$) is derived on the basis of the first order Volterra expansion of the opamp input voltages $V_{\rm d}(\omega)$ and $V_{\rm cm}(\omega)$.

Hence, $V_{\rm d}(\omega)$ and $V_{\rm cm}(\omega)$ are expressed by

$$V_{\rm d}(\omega) = G_{11}(\omega)V^+(\omega) + G_{12}(\omega)V^-(\omega) \tag{3.17}$$

$$V_{\rm cm}(\omega) = G_{21}(\omega)V^+(\omega) + G_{22}(\omega)V^-(\omega). \tag{3.18}$$

With reference to the general linear-feedback configuration shown in Fig. 3.8, which takes into account the finite input admittance and the finite output impedance of the opamp circuit, the frequency domain transfer functions $G_{ij}(\omega)$ take the form

$$G_{11}(\omega) = \frac{D(\omega)\left[Y_1(\omega) + Y_2'(\omega)\right]}{Y_1(\omega) + Y_2'(\omega)\left(1 + A_{\rm d}'(\omega)D(\omega)\right) + Y_3'(\omega)} \tag{3.19}$$

$$G_{12}(\omega) = \frac{-D(\omega)Y_1(\omega)}{Y_1(\omega) + Y_2'(\omega)\left(1 + A_{\rm d}'(\omega)D(\omega)\right) + Y_3'(\omega)} \tag{3.20}$$

$$G_{21}(\omega) = \frac{D(\omega)\left[Y_1(\omega) + Y_2'(\omega)\left(1 + 2A_{\rm d}'(\omega)\right)\right] + Y_3'(\omega)}{2\left[Y_1(\omega) + Y_2'(\omega)\left(1 + A_{\rm d}'(\omega)D(\omega)\right) + 2Y_3'(\omega)\right]} \tag{3.21}$$

$$G_{22}(\omega) = \frac{\left(2 - D(\omega)\right)Y_1(\omega)}{2\left[Y_1(\omega) + Y_2'(\omega)\left(1 + A_{\rm d}'(\omega)D(\omega)\right) + Y_3'(\omega)\right]} \tag{3.22}$$

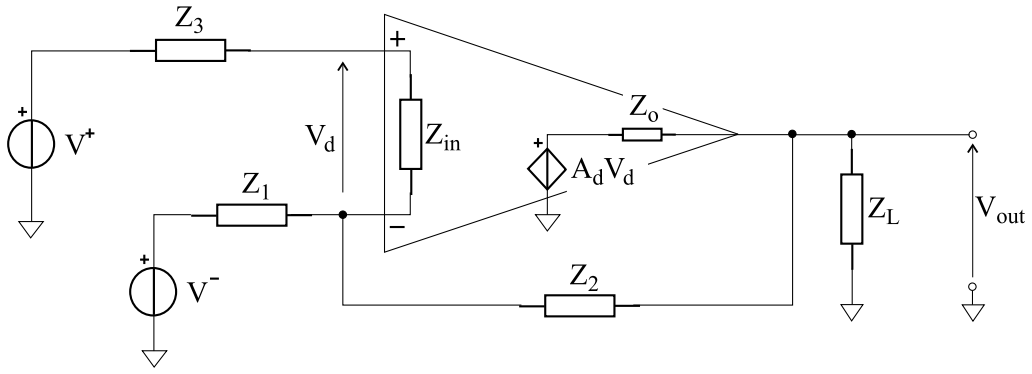


Figure 3.9. General negative feedback opamp configuration.

in which

$$Y_2'(\omega) = \frac{1}{Z_2(\omega) + \frac{1}{Y_\mathrm{o}(\omega)+Y_\mathrm{L}(\omega)}} \tag{3.23}$$

$$Y_3'(\omega) = \frac{1}{Z_3(\omega) + Z_\mathrm{in}(\omega)} \tag{3.24}$$

$$A_\mathrm{d}'(\omega) = A_\mathrm{d}(\omega)\frac{Z_\mathrm{L}(\omega)}{Z_\mathrm{L}(\omega) + Z_\mathrm{o}(\omega)} \tag{3.25}$$

$$D(\omega) = \frac{Z_\mathrm{in}(\omega)}{Z_3(\omega) + Z_\mathrm{in}(\omega)}. \tag{3.26}$$

Now, assuming

$$\begin{aligned} X_1(\omega) &= V^+(\omega) \\ X_2(\omega) &= V^-(\omega) \end{aligned} \tag{3.27}$$

as the input tensor and the opamp output voltage (V_out) as the system output $Y(\omega)$, the Volterra kernels become

$$H^1(\omega_1) = \frac{A_\mathrm{d}(\omega_1)}{1+B(\omega_1)A_\mathrm{d}(\omega_1)}$$
$$H^2(\omega_1) = \frac{(1-B(\omega_1))A_\mathrm{d}(\omega_1)}{1+B(\omega_1)A_\mathrm{d}(\omega_1)}$$

$$\begin{aligned} H^{11}(\omega_1,\omega_2) &= G_{11}(\omega_1)G_{21}(\omega_2)H_0(\omega_2,\omega_1) + G_{21}(\omega_1)G_{11}(\omega_2)H_0(\omega_1,\omega_2) \\ H^{12}(\omega_1,\omega_2) &= G_{11}(\omega_1)G_{22}(\omega_2)H_0(\omega_2,\omega_1) + G_{21}(\omega_1)G_{12}(\omega_2)H_0(\omega_1,\omega_2) \\ H^{21}(\omega_1,\omega_2) &= G_{12}(\omega_1)G_{21}(\omega_2)H_0(\omega_2,\omega_1) + G_{22}(\omega_1)G_{11}(\omega_2)H_0(\omega_1,\omega_2) \\ H^{22}(\omega_1,\omega_2) &= G_{12}(\omega_1)G_{22}(\omega_2)H_0(\omega_2,\omega_1) + G_{22}(\omega_1)G_{12}(\omega_2)H_0(\omega_1,\omega_2). \end{aligned} \tag{3.28}$$

where

$$H_0(\omega_1,\omega_2) = \frac{1}{2}\frac{1}{2I_0}\frac{A_d(\omega_1+\omega_2)}{1+B(\omega_1+\omega_2)A_d(\omega_1+\omega_2)}\frac{2g_\mathrm{m}\mathrm{j}\omega_1 C_\mathrm{T}}{\mathrm{j}\omega_1\left(2C_\mathrm{gs}+C_\mathrm{T}\right)+2g_\mathrm{m}}, \tag{3.29}$$

$$B(\omega) = -\frac{Z_0(\omega)}{Z_0(\omega)+Z_\mathrm{L}'(\omega)}\frac{Z_\mathrm{i}'(\omega)}{Z_\mathrm{i}'(\omega)+Z_2(\omega)}\frac{Z_\mathrm{in}(\omega)}{Z_\mathrm{in}(\omega)+Z_3(\omega)} \tag{3.30}$$

in which

$$Z_\mathrm{i}'(\omega) = \frac{Z_1(\omega)\left(Z_3(\omega)+Z_\mathrm{in}(\omega)\right)}{Z_1(\omega)+Z_3(\omega)+Z_\mathrm{in}(\omega)} \tag{3.31}$$

and

$$Z_\mathrm{L}'(\omega) = \frac{Z_\mathrm{L}(\omega)(Z_2(\omega)+Z_\mathrm{i}'(\omega))}{Z_\mathrm{L}(\omega)+Z_2(\omega)+Z_\mathrm{i}'(\omega)}. \tag{3.32}$$

The previously derived two-input second-order Volterra kernel description of feedback opamp circuits can be employed to derive the expression of the output signal waveform induced by RF interference added to the circuit input nominal signals.

3.2.2 Prediction of RFI-Induced Offset Voltage

The opamp output voltage in the presence of CW RF interference superimposed onto its nominal input signals can be evaluated using Expr. (2.21) on the basis of the Fourier transforms of the input signals and of the Volterra kernels (3.28) as follows

$$\begin{aligned} v_{\mathrm{OUT}}(t) &= \frac{1}{2\pi}\int_{-\infty}^{+\infty} H^1(\omega_1)\,V^+(\omega_1)\,e^{\mathrm{j}\omega_1 t}\mathrm{d}\omega_1 + \\ &+ \frac{1}{2\pi}\int_{-\infty}^{+\infty} H^2(\omega_1)\,V^-(\omega_1)\,e^{\mathrm{j}\omega_1 t}\mathrm{d}\omega_1 + \\ &+ \frac{1}{(2\pi)^2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} H^{11}(\omega_1,\omega_2)\,V^+(\omega_1)\,V^+(\omega_2)\,e^{\mathrm{j}(\omega_1+\omega_2)t}\mathrm{d}\omega_1\mathrm{d}\omega_2 + \\ &+ \frac{1}{(2\pi)^2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} H^{12}(\omega_1,\omega_2)\,V^+(\omega_1)\,V^-(\omega_2)\,e^{\mathrm{j}(\omega_1+\omega_2)t}\mathrm{d}\omega_1\mathrm{d}\omega_2 + \\ &+ \frac{1}{(2\pi)^2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} H^{21}(\omega_1,\omega_2)\,V^-(\omega_1)\,V^+(\omega_2)\,e^{\mathrm{j}(\omega_1+\omega_2)t}\mathrm{d}\omega_1\mathrm{d}\omega_2 + \\ &+ \frac{1}{(2\pi)^2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} H^{22}(\omega_1,\omega_2)\,V^-(\omega_1)\,V^-(\omega_2)\,e^{\mathrm{j}(\omega_1+\omega_2)t}\mathrm{d}\omega_1\mathrm{d}\omega_2. \end{aligned} \tag{3.33}$$

With reference to a DC input signal onto which CW RFI is superimposed (this is the most common operation condition in immunity tests in which RFI is collected by wires and PCB traces), the input tensor takes the form

$$\begin{aligned} V^+(\omega) &= 2\pi\frac{\delta(\omega-\omega_0)+\delta(\omega+\omega_0)}{2}V^+_{\mathrm{pk}} + 2\pi V^+_{\mathrm{DC}}\delta(\omega) \\ V^-(\omega) &= 2\pi\frac{\delta(\omega-\omega_0)+\delta(\omega+\omega_0)}{2}V^-_{\mathrm{pk}} + 2\pi V^-_{\mathrm{DC}}\delta(\omega) \end{aligned} \tag{3.34}$$

in which V^+_{pk} and V^-_{pk} are the peak amplitude of the RF interference superimposed on the DC input voltages V^+_{DC} and V^-_{DC}. Hence, Expr. (3.33) becomes

$$\begin{aligned} v_{\mathrm{out}}(t) &= V^+_{\mathrm{DC}}H^1(0) + V^-_{\mathrm{DC}}H^2(0) + \\ &+ V^+_{\mathrm{pk}}\left|H^1(\omega_0)\right|\cos\left(\omega_0 t + \angle H^1(\omega_0)\right) + V^-_{\mathrm{pk}}\left|H^2(\omega_0)\right|\cos\left(\omega_0 t + \angle H^2(\omega_0)\right) + \\ &+ \frac{V^{+2}_{\mathrm{pk}}}{2}\Re\left\{H^{11}(\omega_0,-\omega_0)\right\} + \frac{V^{+2}_{\mathrm{pk}}}{2}\left|H^{11}(\omega_0,\omega_0)\right|\cos\left(2\omega_0 t + \angle H^{11}(\omega_0,\omega_0)\right) + \\ &+ \frac{V^+_{\mathrm{pk}}V^-_{\mathrm{pk}}}{2}\Re\left\{H^{12}(\omega_0,-\omega_0)\right\} + \frac{V^+_{\mathrm{pk}}V^-_{\mathrm{pk}}}{2}\left|H^{12}(\omega_0,\omega_0)\right|\cos\left(2\omega_0 t + \angle H^{12}(\omega_0,\omega_0)\right) + \\ &+ \frac{V^{-2}_{\mathrm{pk}}}{2}\Re\left\{H^{22}(\omega_0,-\omega_0)\right\} + \frac{V^{-2}_{\mathrm{pk}}}{2}\left|H^{22}(\omega_0,\omega_0)\right|\cos\left(2\omega_0 t + \angle H^{22}(\omega_0,\omega_0)\right) \end{aligned} \tag{3.35}$$

where $\Re\{\cdot\}$ is the real part operator.

In the previous expression the terms at frequency ω_0 and $2\omega_0$ can be neglected since they are out of the opamp circuit bandwidth. As a consequence, Eqn. (3.35) gives that the effect of RFI is an offset in the opamp output voltage which can be written as

$$\begin{aligned} V_{\text{off}} &= \frac{V_{\text{pk}}^{+2}}{2}\Re\left\{H^{11}\left(\omega_0,-\omega_0\right)\right\}+\frac{V_{\text{pk}}^{+}V_{\text{pk}}^{-}}{2}\Re\left\{H^{12}\left(\omega_0,-\omega_0\right)\right\} \\ &+ \frac{V_{\text{pk}}^{-2}}{2}\Re\left\{H^{22}\left(\omega_0,-\omega_0\right)\right\}= \\ &= \left|H_0\left(\omega_0,-\omega_0\right)\right|\left[\Gamma_1\left(\omega_0\right)\frac{V_{\text{pk}}^{+2}}{2}+\Gamma_2\left(\omega_0\right)\frac{V_{\text{pk}}^{+}V_{\text{pk}}^{-}}{2}+\Gamma_3\left(\omega_0\right)\frac{V_{\text{pk}}^{-2}}{2}\right] \end{aligned} \tag{3.36}$$

where

$$H_0(\omega_0,-\omega_0)=\frac{1}{2}\frac{1}{2I_0}\frac{A_d(0)}{1+B(0)A_d(0)}\frac{2g_{\text{m}}\text{j}\omega_0 C_{\text{T}}}{\text{j}\omega_0\left(2C_{\text{gs}}+C_{\text{T}}\right)+2g_{\text{m}}} \tag{3.37}$$

$$\Gamma_1\left(\omega_0\right)=\left|G_{11}(\omega_0)G_{21}(-\omega_0)+G_{21}(\omega_0)G_{11}(-\omega_0)\right|\cos\left(\angle H^{11}\left(\omega_0,-\omega_0\right)\right) \tag{3.38}$$

$$\Gamma_2\left(\omega_0\right)=\left|G_{11}(\omega_0)G_{22}(-\omega_0)+G_{21}(\omega_0)G_{12}(-\omega_0)\right|\cos\left(\angle H^{12}\left(\omega_0,-\omega_0\right)\right) \tag{3.39}$$

$$\Gamma_3\left(\omega_0\right)=\left|G_{12}(\omega_0)G_{22}(-\omega_0)+G_{22}(\omega_0)G_{12}(-\omega_0)\right|\cos\left(\angle H^{22}\left(\omega_0,-\omega_0\right)\right). \tag{3.40}$$

From (3.36) it can be observed that the offset voltage depends on the coefficients Γ_i, that describe the feedback network and on the term $|H_0(\omega_0)|$, which depends on the differential pair design parameters and parasitics. As the term $|H_0(\omega_0)|$ multiplies the overall expression of the offset voltage, the immunity of an opamp to RFI can be enhanced independently of the feedback network, by minimizing this factor. This topic will be covered in the following Chapter, where the enhancement of the immunity of opamp circuits by design is covered. In the following Section the results which are obtained from the Volterra model which has been presented above are compared with the results obtained by experiments.

3.2.3 Model Validation

This section presents a comparison of the predictions obtained using the Volterra series model presented above, experimental results and time domain computer simulation results with reference to a folded cascode opamp connected in the voltage follower configuration.

Device Under Test

In order to validate the proposed Volterra model, the nMOS input folded cascode opamp connected in the voltage follower configuration shown in Fig. 3.10 is considered. This opamp circuit, which is very common in analog systems where high DC gain and large bandwidth are required, shows the electrical characteristics shown in Table 3.1

This circuit has been designed and diffused with reference to the 1μm smart power BCD3s [35] technology process. A photo of the die is given in Fig.3.11.

Table 3.1. Folded Cascode Opamp Electrical Characteristics

Parameter	Unit	Value
Opamp Topology		Folded Cascode
Input Differential Pair		nMOS
Opamp Circuit		Voltage Follower
Power Supply, V_{DD}	V	5
Differential Gain, A_{d}	dB	88
Phase Margin	degrees	90
CMRR	dB	120
PSRR	dB	110
Slew Rate	V/μs	3
Output Current	μA	400
Gain-Bandwidth	MHz	5
Differential Pair Bias Current	μA	10
Differential Pair Transconductance	μS	120

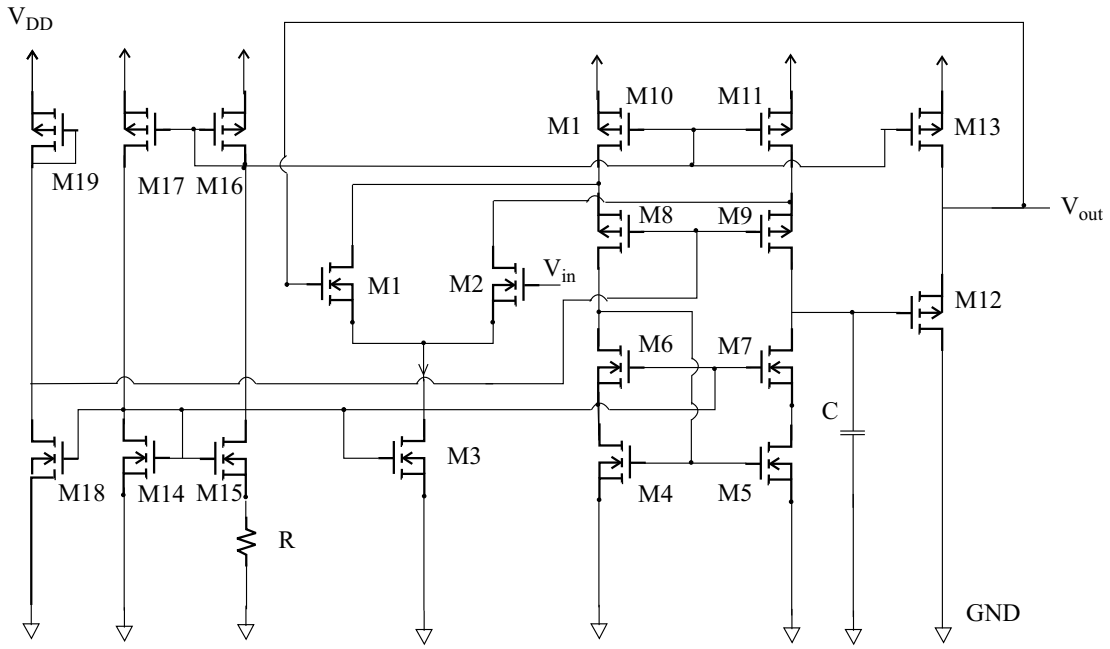


Figure 3.10. Folded Cascode operational amplifier.

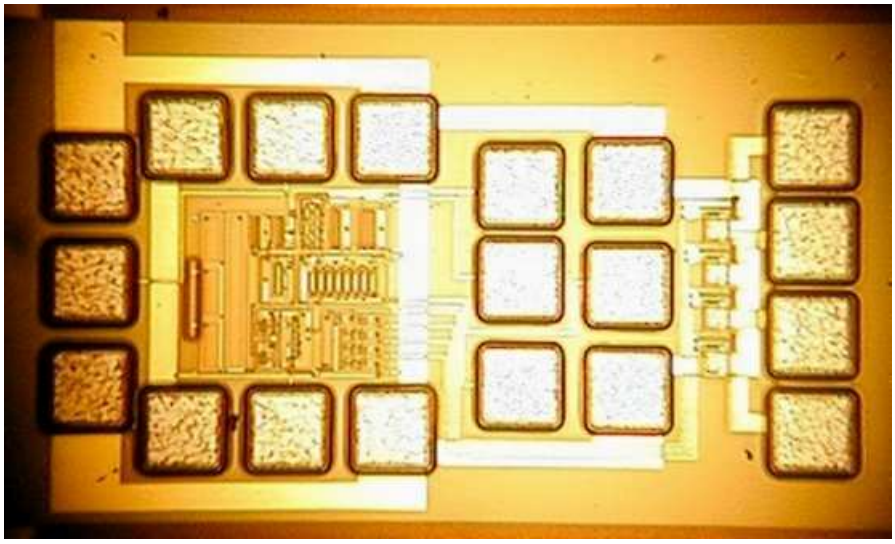


Figure 3.11. Die photo of the Folded Cascode operational amplifier.

Prediction of the Effects of EMI on the DUT

The previously described model is now employed for the prediction of the DC output offset voltage generated in the designed voltage follower circuit driven by a DC input voltage onto which a CW RFI with frequency

$$f_0 = \frac{\omega_0}{2\pi}$$

and amplitude $V_{\rm in}$ is superimposed. Hence, the input signal can be expressed as

$$V^+(\omega) = V_{\rm in} 2\pi \frac{\delta(\omega-\omega_0)+\delta(\omega+\omega_0)}{2} + 2\pi V_{\rm IN}\delta(\omega)$$

and

$$V^-(\omega) = 0.$$

For the voltage follower configuration, expressions (3.19), (3.21) and (3.30) can be simplified as follows

$$G_{11}(\omega) = \frac{D(\omega)}{1+A_{\rm d}(\omega)D(\omega)},$$

$$G_{21}(\omega) = \frac{1}{2}\frac{D(\omega)\left(1+2A_{\rm d}(\omega)\right)}{1+A_{\rm d}(\omega)D(\omega)}$$

and

$$B(\omega) = -\frac{Z_0(\omega)}{Z_0(\omega)+Z_3(\omega)+Z_{\rm in}(\omega)}\frac{Z_{\rm in}(\omega)}{Z_{\rm in}(\omega)+Z_3(\omega)}$$

where $D(\omega)$ is defined in (3.26). Based on the Volterra kernel description (3.28), the opamp output voltage can be derived as shown above. Considering RFI whose frequency is out of the opamp circuit bandwidth ($|A_{\rm d}(\omega_0)| \ll 1$) and assuming that the DC differential amplification is very high ($|A_{\rm d}(0)| \to \infty$), the expression of the output voltage takes the form

$$v_{\rm OUT}(t) \;=\; V_{\rm IN} + V_{\rm in}^2 \frac{g_{\rm m}}{4I_0} \Re\left\{\frac{{\rm j}\omega_0 C_{\rm T}}{{\rm j}\omega_0\left(2C_{\rm gs}+C_{\rm T}\right)+2g_{\rm m}}\right\} \tag{3.41}$$

where it can be noticed that the RFI induced offset voltage in the voltage follower feedback opamp depends on the square of the peak amplitude of the CW interference superimposed onto the voltage follower input multiplied by the factor $\frac{g_{\rm m}}{4I_0}$.

For the designed folded cascode opamp, assuming $g_{\rm m} = 120{\rm mS}$ and $I_0 = 10\mu{\rm A}$, this factor is $\frac{g_{\rm m}}{4I_0} \simeq 3{\rm V}^{-1}$.

The last factor of the second term in (3.41) is frequency dependent: in the designed opamp it increases with frequency up to

$$f_{\rm RF} = \frac{2g_{\rm m}}{2\pi(2C_{\rm gs}+C_{\rm T})} \simeq 30{\rm MHz}.$$

Above this frequency, this factor is almost frequency independent and takes the value

$$\frac{C_{\mathrm{T}}}{2C_{\mathrm{gs}} + C_{\mathrm{T}}} \simeq 0.83.$$

Thus, considering the designed folded cascode opamp connected in the voltage follower configuration with a CW RF interference superimposed onto its input with a frequency above 30MHz and with a peak amplitude of 63mV, the proposed model predicts an offset voltage of about 10mV. The DC output offset voltage prediction obtained by this expression is compared in the following with results of experimental tests.

Experimental Test Setup

On-chip measurements have been carried out using a probe station [36] and employing the test bench shown in Fig.3.12. In this test setup, the input *ground-signal-ground* (GSG) pads of the opamp are contacted by an RF probe [37], which is connected to a bias tee. The remaining two ports of this bias tee are connected to a constant voltage source V_{IN} [38] and to an RF voltage source [39], respectively.

The output GSG pads of the opamp are contacted by an RF probe which is connected to a bias tee as well. The measurement of the output voltage DC component is performed by the DC voltmeter [40] which is connected to the output bias tee while the bias tee RF port is loaded by an impedance $R_{\mathrm{L}} = 50\Omega$. Finally, the DC power supply voltage for the amplifier is provided by a 5V DC voltage source V_{DD} [38].

The DC output offset voltage is obtained as the difference of the DC output voltage measured with and without CW RFI added to the DC input voltage V_{IN}.

It can be observed that the proposed model achieves good agreement with experimental measurements if small amplitude interference is considered and still gives good results as long as the devices which make up the input differential pair work in the saturation region.

Experimental Results

A comparison of the predicted and measured DC output offset voltage versus the interference amplitude and frequency is reported in Fig.3.13 and Fig.3.14. The continuous line refers to the prediction of the new model presented that has been presented above, the squares refer to simulation results obtained by ELDO [25] (time domain analysis) while the circles refer to experimental results.

The proposed model achieves good agreement with experimental data if small amplitude interference is considered and still gives good results as long as the devices which make up the input differential pair work in the saturation region.

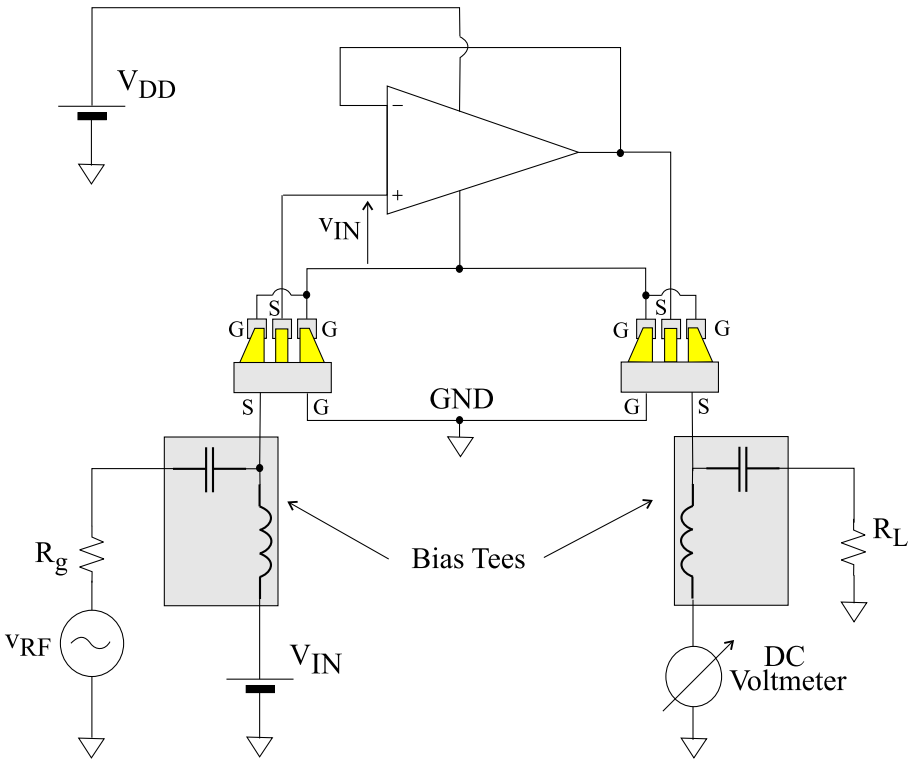


Figure 3.12. Measurement setup.

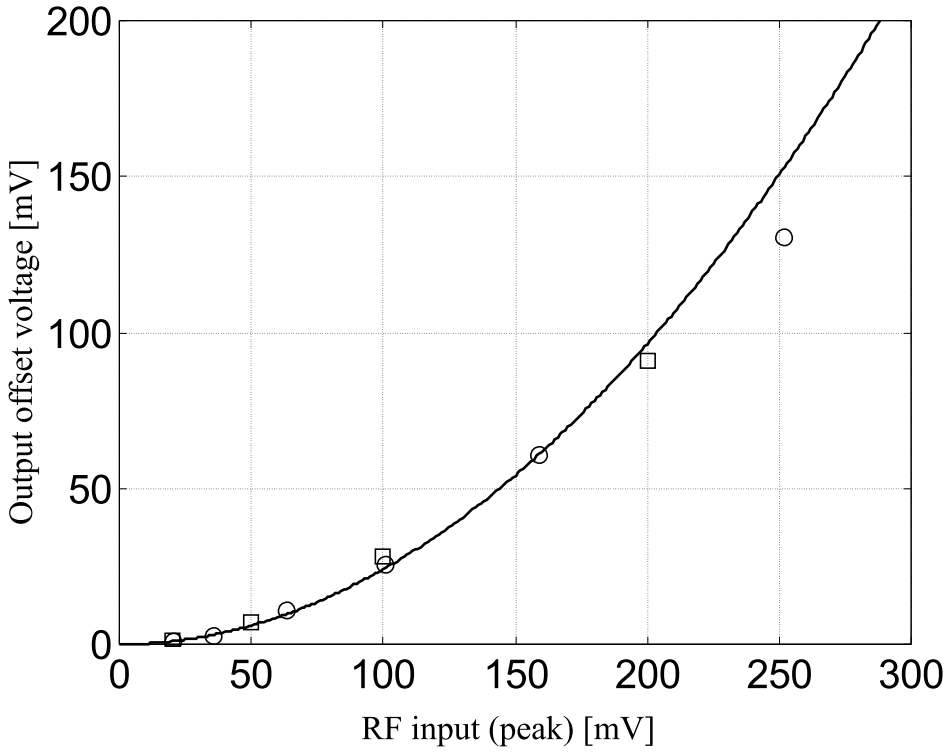


Figure 3.13. Predicted (continuous line), simulated (squares) and measured (circles) RFI induced output voltage shift vs. interference amplitude (constant frequency: 50MHz in the designed Folded Cascode operational amplifier.

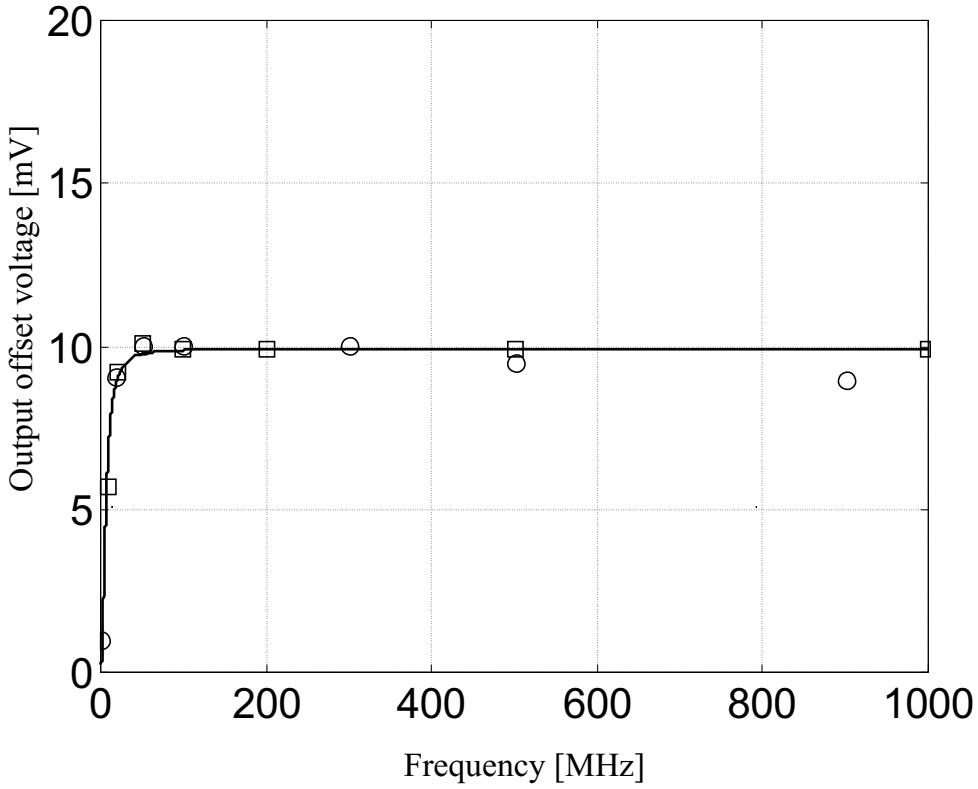


Figure 3.14. Predicted (continuous line), simulated (squares) and measured (circles) RFI induced output voltage shift vs. interference frequency (constant amplitude: 63mV) in the designed Folded Cascode operational amplifier.

3.2.4 Conclusions

The opamp Two-Input Volterra series model which has been presented above shows many features which makes it very useful in the design of opamp circuits immune to EMI. In particular, it relates the RFI-induced offset voltage to design parameters and parasitics in a simple analytical way therefore it can be effectively employed in order to control EMI susceptibility through design.

Nonetheless, it shows some limitations. First, it only considers the effects of RFI which is superimposed onto the opamp circuit input terminals, while the effects of RFI superimposed onto the power supply voltage is not included. Furthermore, it shows the limitations in terms of amplitude of RFI which are due to the Volterra series expansion of the nonlinear characteristics of active devices. The aspects which have been highlighted above will be considered in the following.

3.3 A Three-Input Volterra Series Opamp Model

The Volterra series model which has been presented in the previous Section provides an accurate description of the effects of RFI superimposed onto the opamp input terminals. The aim of this Section is to extend the same approach in order to investigate the effects of RFI superimposed onto the input terminals and/or the power supply rails. To this purpose, after some qualitative considerations on the effects of the disturbances superimposed onto the opamp power supply rails, a Three-Input Second-Order Volterra series model is derived. The predicted effects of RFI onto the opamp power supply rails will be compared with the result of intermodulation measurements. The results of this analysis have been published in [41].

3.3.1 Effects of EMI on the Opamp Power Supply Rails

The demodulation of RFI superimposed onto the input terminals in opamp negative feedback circuits has been traced back to the nonlinear operation of the opamp input differential pair. This assumption, which has been confirmed *a posteriori* by experimental results, was based on two considerations about RF and low frequency signal propagation within an opamp circuit (Section 3.1.1).

When RFI superimposed onto the opamp power supply rails is considered as well, the above hypothesis should be reconsidered. In particular, it can be observed that all the opamp amplifying stages are directly connected to the power supply voltage, therefore each opamp stage is subjected to the same amount of RF disturbance superimposed onto the power supply rail and therefore, each opamp stage can potentially generate the same amount of distortion. Nonetheless, the consideration concerning the propagation of low frequency signals within an opamp circuit in Sec. 3.1.1 still holds, therefore, the assumption that the main contribution to the susceptibility of an opamp circuit to RFI is mainly related to the differential pair nonlinear operation holds even in the presence of RFI superimposed onto the opamp power supply rails.

Furthermore, it should be observed that the distortion which is generated by an amplifying stage in the presence of RFI superimposed *both* onto input terminals and power supply voltages is mostly due to the cross-interaction (intermodulation) between RFI onto the input terminals and onto the power supply rails, i.e., the amount of distortion is proportional to the product of the amplitudes of RFI superimposed onto input and power supply voltages. Therefore, because of the filtering effect on RFI superimposed onto the nominal signal path, the amount of cross-modulation which is generated in the last opamp stages is very low even if the amplitude of RFI superimposed onto the power supply voltage is rather high.

The above considerations lead to the conclusion that the main contribution to the susceptibility of the overall opamp, even in this case, can be traced back to the

input differential pair. Therefore it becomes essential to highlight the effects of RFI superimposed onto the power supply rails in the differential pair operation. To this purpose, in particular, the power supply voltage can no longer be considered as AC ground and the effect of the parasitic capacitance C_{AL} which is connected between the power supply rails and the common source node should be properly taken into account, as shown in the differential pair model in Fig. 3.15 and in its small-signal equivalent in Fig. 3.16.

On the basis of this new differential pair model and on the opamp circuit macromodel shown in Fig.3.2, a three input, Second-Order, Volterra series model is derived in the following.

3.3.2 Model Derivation

In the following, the derivation of the Three-Input Second-Order Volterra series opamp model for EMI susceptibility predictions is presented. This derivation includes the same steps which have been presented in Section 3.2.1: in particular, a differential pair nonlinear model, which also includes the effects of EMI onto the opamp power supply voltage, is firstly derived, then, the differential pair model is employed to derive a model of a complete open-loop opamp and finally the open-loop opamp circuit model is included in a general negative-feedback opamp circuit model.

Differential Pair Model

The derivation of a model for the differential pair nonlinear operation is conceptually similar to what has been presented above with reference to the Two-Input Volterra series Model. In particular, considering the input tensor

$$\begin{aligned} X_1(\omega) &= V_{\mathrm{d}}(\omega) \\ X_2(\omega) &= I_{\mathrm{s}}(\omega) \end{aligned} \tag{3.42}$$

and the differential pair output current $I_{\mathrm{d}}(\omega)$ as the system output $Y(\omega)$, the frequency-domain Volterra kernels up to the second order are again expressed in the form

$$H^1(\omega_1) = \sqrt{2\beta I_0}$$

$$H^2(\omega_1) = 0$$

$$\begin{aligned} H^{11}(\omega_1,\omega_2) &= 0 & H^{12}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}} \\ H^{21}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}} & H^{22}(\omega_1,\omega_2) &= 0. \end{aligned}$$

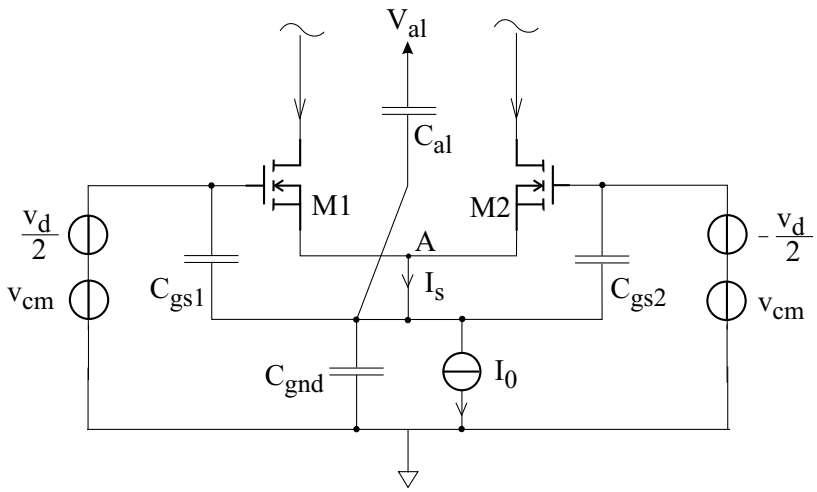


Figure 3.15. Differential Pair Model for the investigation of the effects of RFI onto the power supply rails.

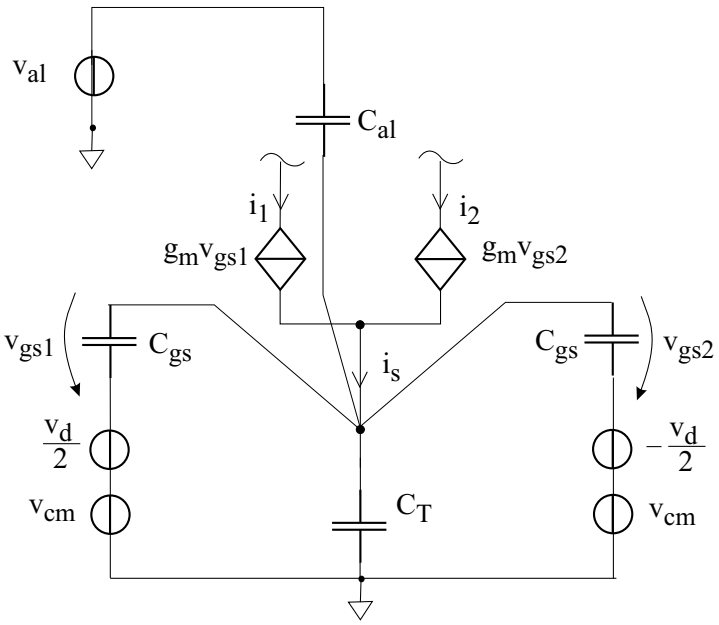


Figure 3.16. Differential Pair Small-Signal Model for the investigation of the effects of RFI onto the power supply rails.

The main difference arises in the expression of the effective differential pair bias current. In the present analysis, the effects on this current of the fluctuations of the power supply voltage should be included in order to derive the differential pair second-order Volterra kernels referred to the tensor

$$\begin{aligned} X_1(\omega) &= V_{\mathrm{d}}(\omega) \\ X_2(\omega) &= V_{\mathrm{cm}}(\omega) \\ X_3(\omega) &= V_{\mathrm{al}}(\omega) \end{aligned} \tag{3.43}$$

which includes the opamp input signals and the power supply voltage.

The first order Volterra series expansion of i_{S} is obtained from the frequency domain analysis of the circuit shown in Fig. 3.16. Such a circuit is the small signal equivalent circuit of the input differential pair.

Hence, the relationship among I_{s}, V_{cm} and V_{al} is given by

$$\begin{aligned} I_{\mathrm{s}}(\omega) &= V_{\mathrm{cm}}(\omega)\frac{2g_{\mathrm{m}}\mathrm{j}\omega(C_{\mathrm{al}}+C_{\mathrm{gnd}})}{\mathrm{j}\omega(2C_{\mathrm{gs}}+C_{\mathrm{al}}+C_{\mathrm{gnd}})+2g_{\mathrm{m}}} + \\ &\qquad + V_{\mathrm{al}}(\omega)\frac{-2g_{\mathrm{m}}\mathrm{j}\omega C_{\mathrm{al}}}{\mathrm{j}\omega(2C_{\mathrm{gs}}+C_{\mathrm{al}}+C_{\mathrm{gnd}})+2g_{\mathrm{m}}} \\ &= V_{\mathrm{cm}}(\omega)\,Y_{\mathrm{cm}}(\omega) + V_{\mathrm{al}}(\omega)\,Y_{\mathrm{al}}(\omega) \end{aligned} \tag{3.44}$$

where C_{gs} is the gate-to-source capacitance of each transistor of the pair.

At this point, the frequency domain Volterra kernels, as a function of the differential pair external inputs, are derived by the substitution of (3.44) in (3.42) and by using the direct expansion method. These kernels take the form

$$\begin{aligned} H^1(\omega_1) &= \sqrt{2\beta I_0} = g_{\mathrm{m}} \\ H^2(\omega_1) &= 0 \\ H^3(\omega_1) &= 0 \\ H^{11}(\omega_1,\omega_2) &= 0 \\ H^{12}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}Y_{\mathrm{cm}}(\omega_2) \\ H^{13}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}Y_{\mathrm{al}}(\omega_2) \\ H^{21}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}Y_{\mathrm{cm}}(\omega_1) \\ H^{22}(\omega_1,\omega_2) &= 0 \\ H^{23}(\omega_1,\omega_2) &= 0 \\ H^{31}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}Y_{\mathrm{al}}(\omega_1) \\ H^{32}(\omega_1,\omega_2) &= 0 \\ H^{33}(\omega_1,\omega_2) &= 0. \end{aligned} \tag{3.45}$$

On the basis of these kernels, which describe the differential pair nonlinear operation, an open-loop opamp Volterra model is derived in the following.

Open-Loop Opamp Model

A CMOS opamp (see Fig.3.2) can be described by a set of Volterra kernels, which can be derived by cascading the three-inputs Volterra system which describes the input differential pair with the linear system that describes the following stages.

With reference to the input tensor $X_k(\omega)$

$$\begin{aligned} X_1(\omega) &= V_{\mathrm{d}}(\omega) \\ X_2(\omega) &= V_{\mathrm{cm}}(\omega) \\ X_3(\omega) &= V_{\mathrm{al}}(\omega) \end{aligned} \tag{3.46}$$

and assuming the opamp output voltage $V_{\mathrm{out}}(\omega)$ as the system output $Y(\omega)$, the following Volterra kernels are derived

$$\begin{aligned} H^1(\omega_1) &= A_{\mathrm{d}}(\omega_1) \\ H^2(\omega_1) &= A_{\mathrm{cm}}(\omega_1) \\ H^3(\omega_1) &= A_{\mathrm{al}}(\omega_1) \end{aligned} \tag{3.47}$$

$$\begin{aligned} H^{11}(\omega_1,\omega_2) &= 0 \\ H^{12}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\tfrac{A_{\mathrm{d}}(\omega_1+\omega_2)}{g_{\mathrm{m}}}Y_{\mathrm{cm}}(\omega_2) \\ H^{13}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\tfrac{A_{\mathrm{d}}(\omega_1+\omega_2)}{g_{\mathrm{m}}}Y_{\mathrm{al}}(\omega_2) \\ H^{21}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\tfrac{A_{\mathrm{d}}(\omega_1+\omega_2)}{g_{\mathrm{m}}}Y_{\mathrm{cm}}(\omega_1) \\ H^{22}(\omega_1,\omega_2) &= 0 \\ H^{23}(\omega_1,\omega_2) &= 0 \\ H^{31}(\omega_1,\omega_2) &= \tfrac{1}{2}\sqrt{\tfrac{\beta}{2I_0}}\tfrac{A_{\mathrm{d}}(\omega_1+\omega_2)}{g_{\mathrm{m}}}Y_{\mathrm{al}}(\omega_1) \\ H^{32}(\omega_1,\omega_2) &= 0 \\ H^{33}(\omega_1,\omega_2) &= 0. \end{aligned}$$

where

$$A_{\mathrm{d}}(\omega) = \frac{V_{\mathrm{out}}(\omega)}{V_{\mathrm{d}}(\omega)}$$

is the opamp differential amplification,

$$A_{\mathrm{cm}}(\omega) = \frac{V_{\mathrm{out}}(\omega)}{V_{\mathrm{cm}}(\omega)}$$

is the opamp common mode amplification and

$$A_{\mathrm{al}}(\omega) = \frac{V_{\mathrm{out}}(\omega)}{V_{\mathrm{al}}(\omega)}$$

is the opamp power supply amplification. Such Volterra kernels provide a complete description of an opamp and they can be employed in the evaluation of distortion phenomena induced by RF interference.

Negative Feedback Opamp Circuit Model

In this section a common CMOS opamp connected in a general negative feedback configuration is considered and it is described in terms of Volterra kernels. The expression of each Volterra kernel is derived on the basis of the Volterra kernels previously derived for the open loop CMOS opamp. The analysis reported in the following refers to the circuit shown in Fig.3.9, where the impedances Z_1-Z_4, the load impedance Z_{L} and the power supply impedance Z_{g} are passive and linear.

As a first step, the input sources v^+, v^- and v'_{al}, which are the elements of the input tensor

$$\begin{aligned} X_1(\omega) &= V^+(\omega) \\ X_2(\omega) &= V^-(\omega) \\ X_3(\omega) &= V'_{\mathrm{al}}(\omega), \end{aligned} \tag{3.48}$$

have to be related with the opamp input signals, which are the elements of the input tensor (3.46). Such a relationship can be derived with reference to the opamp linear model shown in Fig.3.17 because a first order Volterra series expansion of the inputs $V_{\mathrm{d}}(\omega)$, $V_{\mathrm{cm}}(\omega)$ and $V_{\mathrm{al}}(\omega)$ is sufficient to obtain a second order expansion of the opamp output voltage.

The most general linear expressions for the opamp differential input voltage $V_{\mathrm{d}}(\omega)$, the common mode input voltage $V_{\mathrm{cm}}(\omega)$ and for the power supply voltage

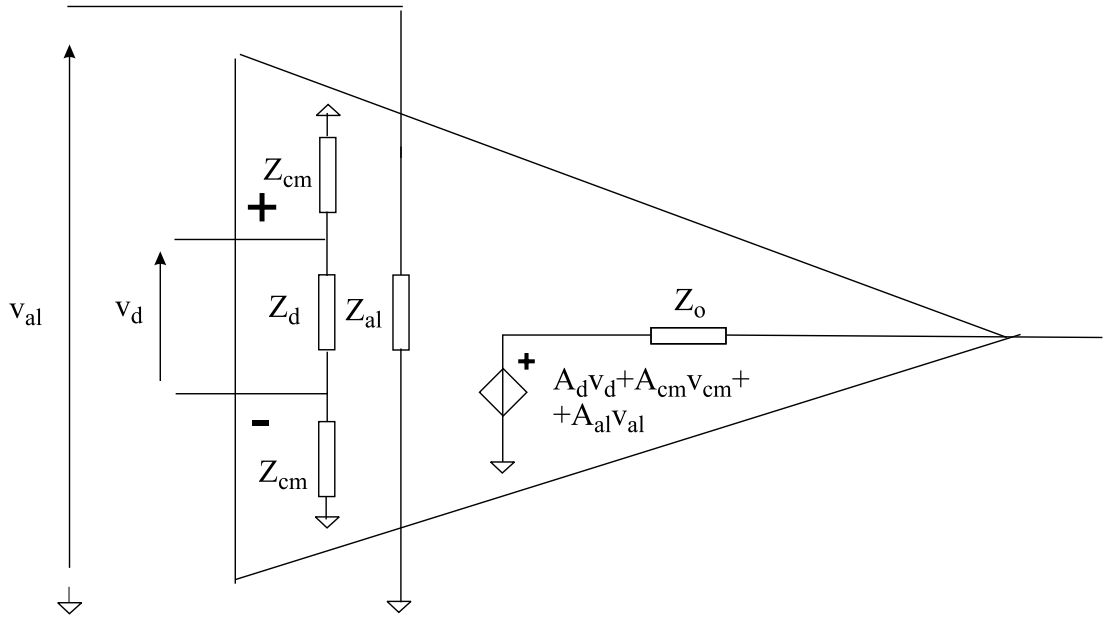


Figure 3.17. Operational Amplifier Linear Model.

$V_{\rm al}(\omega)$ as a function of the external inputs $V^+(\omega)$ and $V^-(\omega)$ and $V'_{\rm al}(\omega)$, can be expressed in the form

$$\begin{aligned} V_{\rm d}(\omega) &= G_{11}(\omega)V^+(\omega) + G_{12}(\omega)V^-(\omega) + G_{13}(\omega)V'_{\rm al}(\omega) \\ V_{\rm cm}(\omega) &= G_{21}(\omega)V^+(\omega) + G_{22}(\omega)V^-(\omega) + G_{23}(\omega)V'_{\rm al}(\omega) \\ V_{\rm al}(\omega) &= G_{31}(\omega)V^+(\omega) + G_{32}(\omega)V^-(\omega) + G_{33}(\omega)V'_{\rm al}(\omega). \end{aligned} \tag{3.49}$$

In this expression the coefficients $G_{\rm ij}(\omega)$ can be derived from the analysis of the circuit shown in Fig.3.9 where the opamp is described by the linear model shown in 3.17. In particular

$$G_{11}(\omega) = \frac{Z_{4\rm e}(\omega)}{Z_3(\omega)+Z_{4\rm e}(\omega)} \frac{D(\omega)\left[Y_{1\rm e}(\omega)+Y'_2(\omega)\right]}{Y_{1\rm e}(\omega)+Y'_2(\omega)\left(1+A'_{\rm d}(\omega)D(\omega)\right)+Y'_3(\omega)} \tag{3.50}$$

$$G_{12}(\omega) = \frac{Z_{\rm cm}(\omega)}{Z_{\rm cm}(\omega)+Z_1(\omega)} \frac{D(\omega)Y_{1\rm e}(\omega)}{Y_{1\rm e}(\omega)+Y'_2(\omega)\left(1+A'_{\rm d}(\omega)D(\omega)\right)+Y'_3(\omega)} \tag{3.51}$$

$$G_{13}(\omega) = B(\omega)A_{\rm al}(\omega) \tag{3.52}$$

$$G_{21}(\omega) = \frac{Z_{4\rm e}(\omega)}{Z_3(\omega)+Z_{4\rm e}(\omega)} \frac{D(\omega)\left[Y_{1\rm e}(\omega)+Y'_2(\omega)\left(1+2A'_{\rm d}(\omega)\right)\right]+Y'_3(\omega)}{2\left[Y_{1\rm e}(\omega)+Y'_2(\omega)\left(1+A'_{\rm d}(\omega)D(\omega)\right)+Y'_3(\omega)\right]} \tag{3.53}$$

$$G_{22}(\omega) = \frac{Z_{\rm cm}(\omega)}{Z_{\rm cm}(\omega)+Z_1(\omega)} \frac{\left(2-D(\omega)\right)Y_{1\rm e}(\omega)}{2\left[Y_{1\rm e}(\omega)+Y'_2(\omega)\left(1+A'_{\rm d}(\omega)D(\omega)\right)+Y'_3(\omega)\right]} \tag{3.54}$$

$$G_{23}(\omega) = \frac{B(\omega)+2B'(\omega)}{2}A_{\rm al}(\omega) \tag{3.55}$$

$$G_{33}(\omega) = \frac{Z_{\rm al}(\omega)}{Z_{\rm al}(\omega)+Z_{\rm g}(\omega)} \tag{3.56}$$

in which

$$Z_{1\rm e}(\omega) = \frac{Z_1(\omega)Z_{\rm cm}(\omega)}{Z_1(\omega)+Z_{\rm cm}(\omega)} \tag{3.57}$$

$$Z_{4\rm e}(\omega) = \frac{Z_4(\omega)Z_{\rm cm}(\omega)}{Z_4(\omega)+Z_{\rm cm}(\omega)} \tag{3.58}$$

$$Z_{3\rm e}(\omega) = \frac{Z_3(\omega)Z_{4\rm e}(\omega)}{Z_3(\omega)+Z_{4\rm e}(\omega)} \tag{3.59}$$

$$Y'_2(\omega) = \frac{1}{Z_2(\omega)+\frac{1}{Y_{\rm o}(\omega)+Y_{\rm L}(\omega)}} \tag{3.60}$$

$$Y'_3(\omega) = \frac{1}{Z_{3\rm e}(\omega)+Z_{\rm d}(\omega)} \tag{3.61}$$

$$A'_{\rm d}(\omega) = A_{\rm d}(\omega)\frac{Z_{\rm L}(\omega)}{Z_{\rm L}(\omega)+Z_{\rm o}(\omega)} \tag{3.62}$$

$$D(\omega) = \frac{Z_{\rm d}(\omega)}{Z_{3\rm e}(\omega)+Z_{\rm d}(\omega)} \tag{3.63}$$

$$B(\omega) = -\frac{Z_{\mathrm{d}}(\omega)}{Z_{\mathrm{d}}(\omega) + Z_{3e}(\omega)} B'(\omega) \tag{3.64}$$

$$B'(\omega) = \frac{Z'_{\mathrm{L}}(\omega)}{Z_0(\omega) + Z'_{\mathrm{L}}(\omega)} \frac{Z'_{\mathrm{i}}(\omega)}{Z'_{\mathrm{i}}(\omega) + Z_2(\omega)} \tag{3.65}$$

$$Z'_{\mathrm{i}}(\omega) = \frac{Z_1(\omega)\left(Z_{3e}(\omega) + Z_{\mathrm{d}}(\omega)\right)}{Z_1(\omega) + Z_{3e}(\omega) + Z_{\mathrm{d}}} \tag{3.66}$$

$$\chi(\omega) = \frac{Z_0(\omega)}{Z_0(\omega) + Z'_{\mathrm{L}}(\omega)} \tag{3.67}$$

and

$$Z'_{\mathrm{L}}(\omega) = \frac{Z_{\mathrm{L}}(\omega)(Z_2(\omega) + Z'_{\mathrm{i}}(\omega))}{Z_{\mathrm{L}}(\omega) + Z_2(\omega) + Z'_{\mathrm{i}}(\omega)}. \tag{3.68}$$

In addition $G_{31}(\omega) = G_{32}(\omega) = 0$ because the opamp power supply voltage does not depend on the opamp input voltages.

Therefore, the kernels up to the second order can be expressed as

$$\begin{aligned} H^1(\omega_1) &= \frac{A_{\mathrm{d}}(\omega_1) + A_0(\omega_1)}{1 + B(\omega_1)A_{\mathrm{d}}(\omega_1)} + A_{\mathrm{cm}}(\omega_1)G_{21}(\omega_1)\chi(\omega_1) \\ H^2(\omega_1) &= \frac{(B(\omega_1) - 1)A_{\mathrm{d}}(\omega_1)}{1 + B(\omega_1)A_{\mathrm{d}}(\omega_1)} + A_{\mathrm{cm}}(\omega_1)G_{22}(\omega_1)\chi(\omega_1) \\ H^3(\omega_1) &= A_{\mathrm{al}}(\omega_1)G_{33}(\omega_1) \end{aligned} \tag{3.69}$$

$$\begin{aligned} H^{11}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{11}(\omega_1)G_{21}(\omega_2)Y_{\mathrm{cm}}(\omega_2) + G_{21}(\omega_1)G_{11}(\omega_2)Y_{\mathrm{cm}}(\omega_1)\right] \\ H^{12}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{12}(\omega_1)G_{21}(\omega_2)Y_{\mathrm{cm}}(\omega_2) + G_{11}(\omega_1)G_{22}(\omega_2)Y_{\mathrm{cm}}(\omega_2)\right] \\ H^{13}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{11}(\omega_1)G_{33}(\omega_2)Y_{\mathrm{al}}(\omega_2) + G_{11}(\omega_1)G_{23}(\omega_2)Y_{\mathrm{cm}}(\omega_2)\right] \\ H^{21}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{12}(\omega_2)G_{21}(\omega_1)Y_{\mathrm{cm}}(\omega_1) + G_{11}(\omega_2)G_{22}(\omega_1)Y_{\mathrm{cm}}(\omega_1)\right] \\ H^{22}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{12}(\omega_1)G_{22}(\omega_2)Y_{\mathrm{cm}}(\omega_2) + G_{12}(\omega_2)G_{22}(\omega_1)Y_{\mathrm{cm}}(\omega_1)\right] \\ H^{23}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{12}(\omega_1)G_{33}(\omega_2)Y_{\mathrm{al}}(\omega_2) + G_{12}(\omega_1)G_{23}(\omega_2)Y_{\mathrm{cm}}(\omega_2)\right] \\ H^{31}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{11}(\omega_2)G_{33}(\omega_1)Y_{\mathrm{al}}(\omega_1) + G_{11}(\omega_2)G_{23}(\omega_1)Y_{\mathrm{cm}}(\omega_1)\right] \\ H^{32}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{12}(\omega_2)G_{33}(\omega_1)Y_{\mathrm{al}}(\omega_1) + G_{12}(\omega_2)G_{23}(\omega_1)Y_{\mathrm{cm}}(\omega_1)\right] \\ H^{32}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{12}(\omega_2)G_{33}(\omega_1)Y_{\mathrm{al}}(\omega_1) + G_{12}(\omega_2)G_{23}(\omega_1)Y_{\mathrm{cm}}(\omega_1)\right] \\ H^{33}(\omega_1,\omega_2) &= H_0(\omega_1+\omega_2)\left[G_{13}(\omega_1)G_{33}(\omega_2)Y_{\mathrm{al}}(\omega_2) + G_{13}(\omega_1)G_{23}(\omega_2)Y_{\mathrm{cm}}(\omega_2) + \right. \\ &\quad \left. + G_{13}(\omega_2)G_{33}(\omega_1)Y_{\mathrm{al}}(\omega_1) + G_{13}(\omega_2)G_{23}(\omega_1)Y_{\mathrm{cm}}(\omega_1)\right] \end{aligned}$$

where

$$A_0(\omega) = \frac{Z_{4e}(\omega)}{Z_3(\omega) + Z_{4e}(\omega)} \frac{Z_{1e}(\omega) \parallel (Z_2(\omega) + Z_0(\omega) \parallel Z_L(\omega))}{Z_d(\omega) + Z_{1e}(\omega) \parallel (Z_2(\omega) + Z_0(\omega) \parallel Z_L(\omega))} \frac{Z_L(\omega) \parallel Z_0(\omega)}{Z_2(\omega) + Z_L(\omega) \parallel Z_0} \tag{3.70}$$

$$H_0(\omega) = \frac{1}{4I_0} \left(1 + \frac{Z_3(\omega)}{Z_4(\omega)}\right) \left[\frac{A_d(\omega) + A_0(\omega)}{1 + B(\omega)A_d(\omega)} + A_{cm}(\omega)G_{21}(\omega)\chi(\omega)\right]. \tag{3.71}$$

In the following the Volterra kernels derived above are employed to investigate the effects of RF interference added simultaneously to the opamp input nominal signals and to the power supply voltage.

3.3.3 Demodulation of RFI in Feedback Opamps

The case of two-tone RF interference added simultaneously to a feedback opamp input nominal signals and to the power supply voltage is now considered. For such a case, the expression of the DC output offset voltage and that of the intermodulation products, which are located inside the opamp bandwidth, are derived. The analysis of such a specific case highlights some criteria that are useful to design opamp immune to EMI. These criteria will be discussed more deeply in the next Chapter.

Intermodulation Products

Each input port of the circuit shown in Fig.3.9 is driven by a two tone RF signal superimposed onto a DC voltage. The angular frequencies of each tone (ω_1 and ω_2) are chosen so that $|A_{\mathrm{d}}(\omega_1)| \ll 1$ and $|A_{\mathrm{d}}(\omega_2)| \ll 1$ while $|A_{\mathrm{d}}(\omega_1' - \omega_2)| \gg 1$ i.e. ω_1 and ω_2 are out of the opamp bandwidth while their difference is inside the bandwidth.

In particular, the input tensor can be written in the form

$$\begin{aligned}
V^+ &= 2\pi\delta(\omega)V_{\mathrm{DC}}^+ + \\
&+ 2\pi\frac{\delta(\omega-\omega_0)\mathrm{e}^{-\mathrm{j}\varphi_{11}} + \delta(\omega+\omega_0)\mathrm{e}^{\mathrm{j}\varphi_{11}}}{2}V_{11} + \\
&+ 2\pi\frac{\delta(\omega-\omega_0')\mathrm{e}^{-\mathrm{j}\varphi_{21}} + \delta(\omega+\omega_0')\mathrm{e}^{\mathrm{j}\varphi_{21}}}{2}V_{21} \\
V^- &= 2\pi\delta(\omega)V_{\mathrm{DC}}^- + \\
&+ 2\pi\frac{\delta(\omega-\omega_0)\mathrm{e}^{-\mathrm{j}\varphi_{12}} + \delta(\omega+\omega_0)\mathrm{e}^{\mathrm{j}\varphi_{12}}}{2}V_{12} + \\
&+ 2\pi\frac{\delta(\omega-\omega_0')\mathrm{e}^{-\mathrm{j}\varphi_{22}} + \delta(\omega+\omega_0')\mathrm{e}^{\mathrm{j}\varphi_{22}}}{2}V_{22} \\
V_{\mathrm{al}} &= 2\pi\delta(\omega)V_{\mathrm{al,DC}} + \\
&+ 2\pi\frac{\delta(\omega-\omega_0)\mathrm{e}^{-\mathrm{j}\varphi_{13}} + \delta(\omega+\omega_0)\mathrm{e}^{\mathrm{j}\varphi_{13}}}{2}V_{13} + \\
&+ 2\pi\frac{\delta(\omega-\omega_0')\mathrm{e}^{-\mathrm{j}\varphi_{23}} + \delta(\omega+\omega_0')\mathrm{e}^{\mathrm{j}\varphi_{23}}}{2}V_{23}
\end{aligned} \tag{3.72}$$

where V_{ij} are the peak amplitudes of the RF interference components at frequency ω_0 (for $i = 1$) or ω_0' (for $i = 2$) superimposed on voltage V^+ ($j = 1$), V^- ($j = 2$) or V_{al} ($j = 3$), φ_{ij} are the phase shifts of the previous components with respect to an arbitrary phase reference and V_{DC}^+, V_{DC}^- and $V_{\mathrm{al,DC}}$ are respectively the nominal DC values of the voltages V^+, V^- and V_{al}. In the following, the frequencies of the two tones are assumed to be closely spaced, i.e. $\omega_0 \simeq \omega_0' \simeq \omega^*$ and the fluctuation of each function of interest is neglected ($f(\omega_0) \simeq f(\omega_0') \simeq f(\omega^*)$).

Both the DC output offset voltage and the demodulated output signal can be derived by using the expressions of the input signals given in (3.72). In particular, the DC output offset voltage (V_{off}) can be expressed in the form

$$\begin{aligned} V_{\text{off}} &= \frac{1}{2}\left|H_{\text{cm}}(0,\omega^*)\right|\left|S_1\right|\cos\left(\angle H_{\text{cm}}(0,\omega^*)S_1\right) \\ &+ \frac{1}{2}\left|H_{\text{al}}(0,\omega^*)\right|\left|S_2\right|\cos\left(\angle H_{\text{al}}(0,\omega^*)S_2\right) \end{aligned} \tag{3.73}$$

in which

$$S_1 = \sum_{i=1}^{3}\sum_{j=i}^{3}\left(V_{1\text{i}}V_{1\text{j}}\Gamma_{ij}(\omega^*)\text{e}^{\text{j}(\varphi_{1i}-\varphi_{1j})} + V_{2\text{i}}V_{2\text{j}}\Gamma_{ij}(\omega^*)\text{e}^{\text{j}(\varphi_{2i}-\varphi_{2j})}\right) \tag{3.74}$$

$$S_2 = \sum_{i=1}^{3}\sum_{j=i}^{3}\left(V_{1\text{i}}V_{1\text{j}}\Gamma'_{ij}(\omega^*)\text{e}^{\text{j}(\varphi_{1i}-\varphi_{1j})} + V_{2\text{i}}V_{2\text{j}}\Gamma'_{ij}(\omega^*)\text{e}^{\text{j}(\varphi_{2i}-\varphi_{2j})}\right) \tag{3.75}$$

$$\begin{aligned} \Gamma_{11} &= G_{11}G_{21} \\ \Gamma_{12} &= G_{12}G_{21} + G_{11}G_{22} \\ \Gamma_{13} &= G_{11}G_{23} \\ \Gamma_{22} &= G_{12}G_{22} \\ \Gamma_{23} &= G_{12}G_{23} \\ \Gamma_{33} &= G_{13}G_{23} \end{aligned}$$

$$\begin{aligned} \Gamma'_{11} &= 0 \\ \Gamma'_{12} &= 0 \\ \Gamma'_{13} &= G_{11}G_{33} \\ \Gamma'_{22} &= 0 \\ \Gamma'_{23} &= G_{12}G_{33} \\ \Gamma'_{33} &= G_{13}G_{33} \end{aligned}$$

In the same expression the term

$$\begin{aligned} H_{\text{cm}}(\omega_1,\omega_2) &= \frac{1}{4I_0}\frac{2g_{\text{m}}\text{j}\omega_2(C_{\text{al}}+C_{\text{gnd}})}{\text{j}\omega_2\left(2C_{\text{gs}}+C_{\text{al}}+C_{\text{gnd}}\right)+2g_{\text{m}}} \\ &\quad \left(1+\frac{Z_3(\omega_1)}{Z_4(\omega_1)}\right)\left[\frac{A_{\text{d}}(\omega_1)+A_0(\omega_1)}{1+B(\omega_1)A_{\text{d}}(\omega_1)} + A_{\text{cm}}(\omega_1)G_{21}(\omega_1)\chi(\omega_1)\right] \\ &\simeq \frac{1}{4I_0}\frac{2g_{\text{m}}\text{j}\omega_2(C_{\text{al}}+C_{\text{gnd}})}{\text{j}\omega_2\left(2C_{\text{gs}}+C_{\text{al}}+C_{\text{gnd}}\right)+2g_{\text{m}}}\left(1+\frac{Z_3(\omega_1)}{Z_4(\omega_1)}\right)\frac{A_{\text{d}}(\omega_1)}{1+B(\omega_1)A_{\text{d}}(\omega_1)} \end{aligned} \tag{3.76}$$

and

$$
\begin{aligned}
H_{\mathrm{al}}(\omega_1,\omega_2) &= \frac{1}{4I_0}\frac{-2g_{\mathrm{m}}\mathrm{j}\omega_2 C_{\mathrm{al}}}{\mathrm{j}\omega_2\left(2C_{\mathrm{gs}}+C_{\mathrm{al}}+C_{\mathrm{gnd}}\right)+2g_{\mathrm{m}}} \\
&\quad \left(1+\frac{Z_3(\omega_1)}{Z_4(\omega_1)}\right)\left[\frac{A_{\mathrm{d}}(\omega_1)+A_0(\omega_1)}{1+B(\omega_1)A_{\mathrm{d}}(\omega_1)}+A_{\mathrm{cm}}(\omega_1)G_{21}(\omega_1)\chi(\omega_1)\right] \\
&\simeq \frac{1}{4I_0}\frac{-2g_{\mathrm{m}}\mathrm{j}\omega_2 C_{\mathrm{al}}}{\mathrm{j}\omega_2\left(2C_{\mathrm{gs}}+C_{\mathrm{al}}+C_{\mathrm{gnd}}\right)+2g_{\mathrm{m}}}\left(1+\frac{Z_3(\omega_1)}{Z_4(\omega_1)}\right)\frac{A_{\mathrm{d}}(\omega_1)}{1+B(\omega_1)A_{\mathrm{d}}(\omega_1)}
\end{aligned}
\tag{3.77}
$$

multiply each term of (3.73) and they depend on circuit design parameters in a straightforward way. For this reason, if the magnitudes of $H_{\mathrm{cm}}(\omega_1,\omega_2)$ and $H_{\mathrm{al}}(\omega_1,\omega_2)$ are kept to a minimum by a proper circuit design, an improvement of the immunity of any opamp circuit to RF interference can be achieved, independently on the particular feedback configuration employed and on the different amplitudes or reciprocal phase shifts of the different RFI components superimposed on V^+, V^- and V_{al}.

In a similar way, the intermodulation products, with frequency $\omega_0-\omega_0'$, can be expressed in the time domain as follows

$$
\begin{aligned}
v_{\mathrm{INT}}(t) &= |H_{\mathrm{cm}}(\omega_{\mathrm{d}},\omega^*)|\,|S_1|\cos\left(\omega_{\mathrm{d}}t+\angle H_{\mathrm{cm}}(\omega_{\mathrm{d}},\omega^*)S_1\right)+ \\
&+ |H_{\mathrm{al}}(\omega_{\mathrm{d}},\omega^*)|\,|S_2|\cos\left(\omega_{\mathrm{d}}t+\angle H_{\mathrm{al}}(\omega_{\mathrm{d}},\omega^*)S_2\right)
\end{aligned}
$$

where

$$\omega_d=\omega_0-\omega_0'.$$

The magnitudes of the terms $H_{\mathrm{cm}}(\omega_1,\omega_2)$ and $H_{\mathrm{al}}(\omega_1,\omega_2)$ multiply once again each contribution to the overall peak amplitude of the intermodulation products. Thus, if the magnitude of such terms is reduced by a proper circuit design, also the amplitude of intermodulation products are reduced. The aspects related with the reduction of the susceptibility to EMI by design will be presented in detail in the next Chapter.

3.3.4 Model Validation

This section shows the results of intermodulation measurements performed on a CMOS folded cascode opamp connected in the voltage follower configuration in the presence of CW RF signals added simultaneously to the nominal input signal and to the power supply voltage. The results of these measurements are compared with the model predictions.

The Device Under Test

A CMOS folded cascode opamp connected in the voltage follower configuration was chosen as a device under test (DUT). This circuit, whose schematic is shown in Fig. 3.10, is made up by a nMOS differential pair input stage (M1-M3) which is followed by a cascode gain stage (M4-M11) and by an output current-gain source follower stage (M12-M13). All the DC bias voltages, which are necessary for the operation of the circuit, are provided by the bias network (M14-M19). An on-chip compensation capacitor is connected between the high impedance output of the gain stage and ground (C).

Such a circuit was designed and fabricated in a standard BiCMOS technology process and the electrical characteristic of this opamp are reported in Table 3.2.

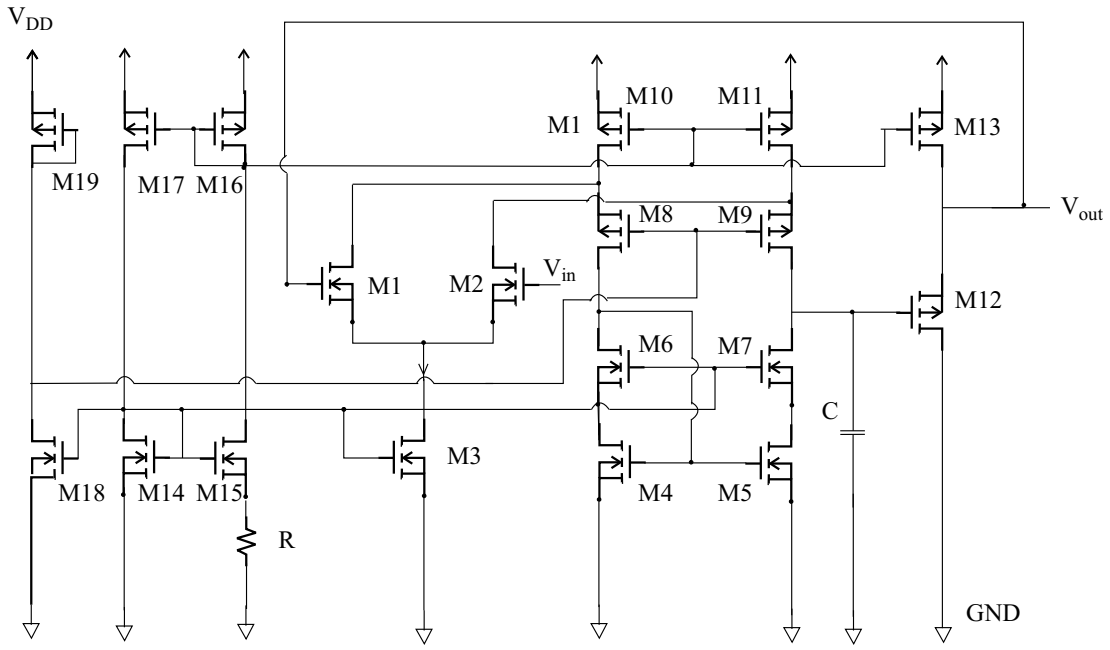


Figure 3.18. Designed Folded Cascode Operational Amplifier.

Parameter	Value
Differential Amplification A_d	88dB
Phase Margin	90°
CMRR	120dB
PSRR	110dB
Slew Rate	3 V/μs
Maximum Output Current	400μA
Gain-Bandwidth Product	5MHz

Table 3.2. Electrical characteristics of the designed Folded Cascode opamp.

Prediction of RFI Demodulation in the DUT

The Three-Input Volterra series model of a general feedback opamp which has been derived above is employed to derive the expression of the intermodulation product which is added to the nominal output voltage of the voltage follower described in Section 3.3.4 when CW RF signals with different frequencies are superimposed to the input nominal signal and to the power supply voltage.

With reference to the voltage follower circuit shown in Fig. 3.19, the input tensor has the form

$$V^{+} = 2\pi \frac{\delta(\omega-\omega_0)+\delta(\omega+\omega_0)}{2} V_{\text{in}} + 2\pi\delta(\omega)V_{\text{IN}} \tag{3.78}$$

$$V^{-} = 0 \tag{3.79}$$

$$V'_{\text{al}} = 2\pi \frac{\delta(\omega-\omega'_0)+\delta(\omega+\omega'_0)}{2} V_{\text{dd}} + 2\pi\delta(\omega)V_{\text{DD}}, \tag{3.80}$$

only the second order kernels H^{11}, H^{13}, H^{31} and H^{33} have to be taken into account. Among these kernels, H^{11} and H^{33} are responsible of the DC output voltage shift, while the kernels H^{13} and H^{31}, which are the same kernel with permuted variables, are responsible of the cross modulation terms.

Exprs. (3.50), (3.55) and (3.56) can be simplified for the voltage follower configuration as

$$G_{11} = \frac{Y_{cm}+Y_0+Y_{\text{L}}}{Y_{cm}+(Y_{cm}+Y_0+Y_{\text{L}})(1+A_{\text{d}})+Y_{\text{d}}}, \tag{3.81}$$

$$G_{23} = \frac{1}{2}A_{\text{al}}\frac{Z'_{\text{L}}}{Z'_{\text{L}}+Z_0}, \tag{3.82}$$

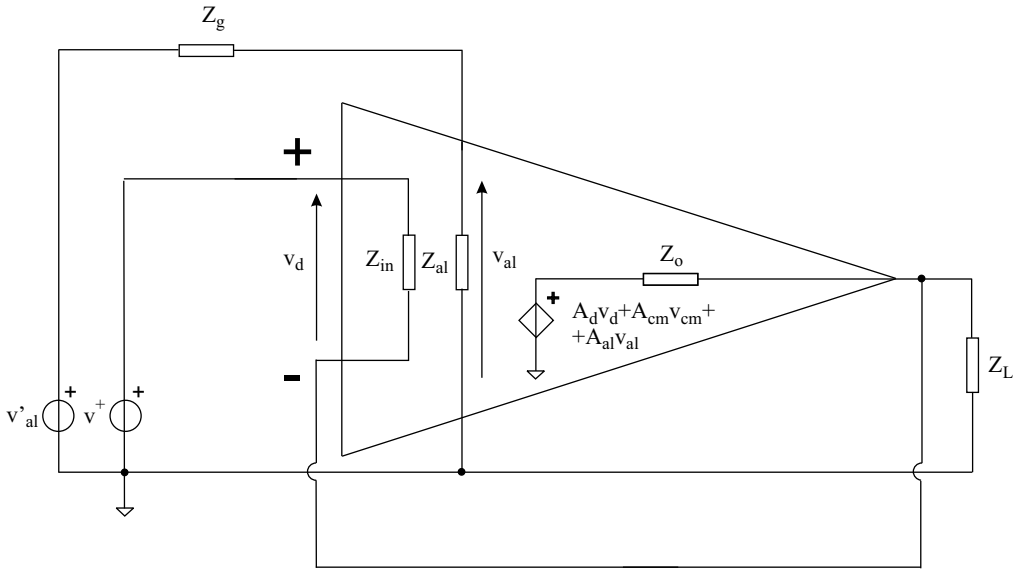


Figure 3.19. Voltage follower operational amplifier configuration.

$$G_{33} = \frac{Z_{\rm al}}{Z_{\rm al} + Z_{\rm g}} \tag{3.83}$$

where

$$Z'_{\rm L} = \frac{Z_{\rm L} Z_{\rm d}}{Z_{\rm L} + Z_{\rm d}}.$$

Now, the expressions of H_{13}, H_{31} and the input tensor (3.79) are employed in (2.21) to derive the the intermodulation product:

$$\begin{aligned} V_{\rm out,int} &= \frac{V_{\rm in} V_{\rm dd}}{2} \left| H_0(\omega'_0 - \omega_0) \right| \\ &\quad \left| \left[G_{11}(\omega_0) G_{33}(\omega'_0) Y_{\rm al}(\omega'_0) + G_{11}(\omega_0) G_{23}(-\omega'_0) Y_{\rm cm}(\omega'_0) \right] \right|. \end{aligned} \tag{3.84}$$

Since the opamp described in (3.3.4) shows a power supply supply amplification $A_{\rm al} \ll 1$ the second term of (3.84) in the square brackets is negligible if compared to the first one and (3.84) becomes

$$\begin{aligned} V_{\rm out,int} &= \frac{V_{\rm in} V_{\rm dd}}{2} \left| H_0(\omega'_0 - \omega_0) G_{11}(\omega_0) G_{33}(\omega'_0) Y_{\rm al}(\omega'_0) \right| = \\ &\simeq \frac{V_{\rm in} V_{\rm dd}}{2} \frac{1}{4 I_0} \left| \frac{Z_{\rm al}(\omega'_0)}{Z_{\rm al}(\omega'_0) + Z_{\rm g}(\omega'_0)} \right| \frac{2 g_{\rm m} \omega'_0 C_{\rm al}}{\sqrt{\omega'^2_0 \left(2C_{\rm gs} + C_{\rm al} + C_{\rm gnd}\right)^2 + 4 g^2_{\rm m}}}. \end{aligned} \tag{3.85}$$

This expression has been derived assuming $|Y_{\rm d}(\omega_0)| \ll |Y_0(\omega_0) + Y_{\rm L}(\omega_0)|$ and considering $|A_{\rm cm}(\omega'_0 - \omega_0)| \ll 1$. Furthermore, the frequencies of the RF signals superimposed on the opamp nominal input voltage and on the power supply voltage are assumed to be out of the opamp bandwidth ($|A_{\rm d}(\omega_0)| \ll 1$, $|A_{\rm d}(\omega'_0)| \ll 1$), while their difference $\omega'_0 - \omega_0$ is supposed to be within the opamp bandwidth ($|A_{\rm d}(\omega'_0 - \omega_0)| \gg 1$).

The predictions on the amplitude of RFI-induced intermodulation products obtained from (3.85) will be compared in the following with the results of on-chip measurements which have been carried out on the DUT.

Measurement Results

The effect of RF interference on the operation of such a circuit was experimentally characterized by the superposition of a CW RF signal with angular frequency ω_0 on the voltage follower input nominal voltage and a CW RF signal with angular frequency ω'_0 on the DC power supply voltage. In particular the stimuli are expressed as

$$v^+(t) = V_{\rm IN} + V_{\rm in} \cos(\omega_0 t) \tag{3.86}$$

$$v'_{\rm al}(t) = V_{\rm DD} + V_{\rm dd} \cos(\omega'_0 t) \tag{3.87}$$

where $V_{\rm IN}$ and $V_{\rm DD}$ are respectively the nominal DC values of the input and of the power supply voltage while $V_{\rm in}$ and $V_{\rm dd}$ are the peak amplitudes of the RF signals superimposed on the input signal and on the power supply voltage.

Two RF signals of different frequency are selected in order to perform the measurement of the intermodulation products, which are superimposed to the output nominal signal. This choice is preferable to the measurement of the DC output offset voltage, which is induced by two CW RF signals with the same frequency, because in the last case such a DC output offset voltage depends on the relative phase shift of the two RF signals. This fact, makes the measurement of the DC output offset voltage scarcely repeatable.

The intermodulation product was measured by the test setup shown in Fig.3.20 which includes a microwave probe station [36], two RF signal sources [39] whose impedance is $R_{\rm g} = 50\Omega$, a multi-channel DC power supply [38] and a spectrum analyzer [42]. In this bench, the opamp input *ground-signal-ground* (GSG) pads on wafer (see Fig. 3.20) are contacted by an RF probe [37], which is connected to the output port of a bias tee. The bias tee DC input port is connected to a channel of the DC power supply (voltage $V_{\rm IN}$), while the bias tee RF input port is connected to the RF source ($V_{\rm in}$). In this way the input signal (3.86) is obtained. Similarly, the power supply GSG pads of the opamp (see Fig.3.20) are contacted by an RF probe which is connected to the output port of a bias tee. The bias tee DC input port is connected to a channel of the DC power supply (voltage $V_{\rm DD}$), while the bias tee RF input port is connected to the RF source ($V_{\rm dd}$). Finally, the opamp output pad is contacted by a low-frequency probe which is connected via a DC block capacitor to the input of a spectrum analyzer. A low frequency probe has been employed in order to measure the output voltage as, it has been previously verified by RF measurements that the amplitude of RFI superimposed onto the opamp output voltage is very low. Therefore, the presence of the low frequency probe does not affect RFI propagation in the opamp circuit. Furthermore, the band of the low frequency probe is large enough for the measurement of the low frequency (200kHz) intermodulation products which are considered in the following.

The measurement of the intermodulation product generated in the voltage follower was performed for $f_0 = 200$MHz, $f_0' = 200.2$MHz and $f_0 = 500$MHz, $f_0' = 500.2$MHz. In both cases the frequency spacing is 200kHz and it is within the opamp bandwidth.

The amplitude of the intermodulation product on the opamp output voltage was measured by the spectrum analyzer versus the amplitude of the RF signals injected on the voltage follower input port and on the power supply port. In particular, Fig. 3.21 and 3.22 show the amplitude of the intermodulation product (peak value) versus the amplitude (peak value) of the RF signal superimposed on the opamp power supply voltage for several values of the amplitude (peak value) of the RF signal superimposed on the opamp input terminal.

The same figures show the prediction of the intermodulation product amplitude, which has been predicted by the Three-Input Volterra series model presented above.

It can be observed that the proposed approach achieves a good agreement with experimental measurements if small amplitude interference is considered and it gives still good results as long as the transistors which make up the input differential pair work in the saturation region. The disagreement between model prediction and experimental results for a high level of injected RFI is due to high order distortion which is not taken into account in the second-order Volterra series analysis.

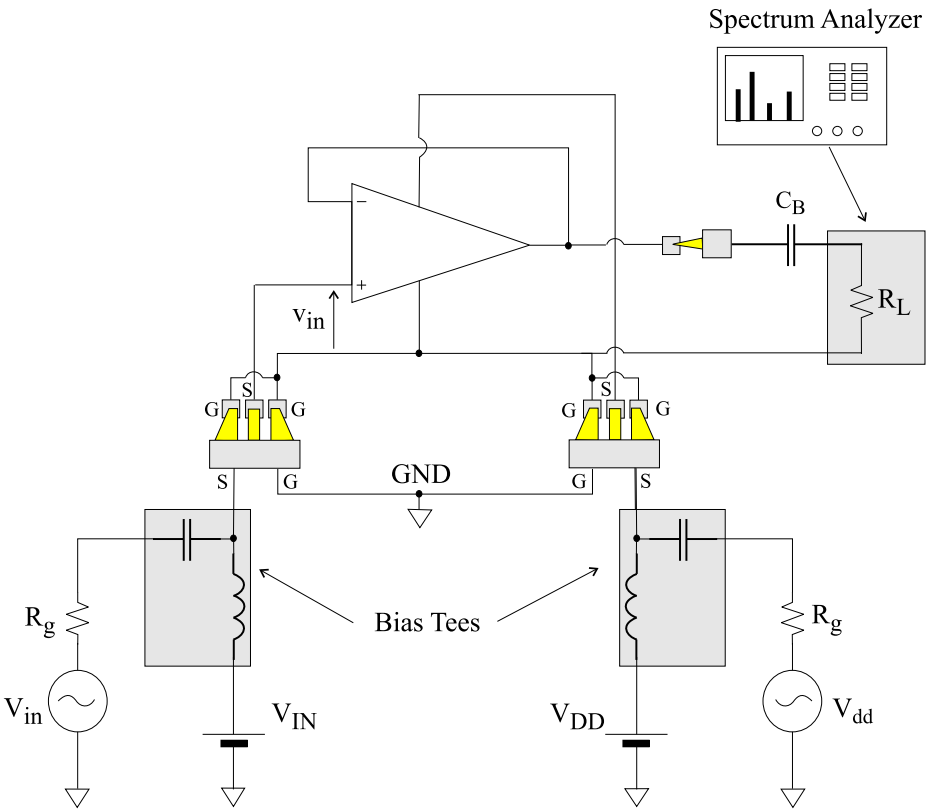


Figure 3.20. Measurement setup.

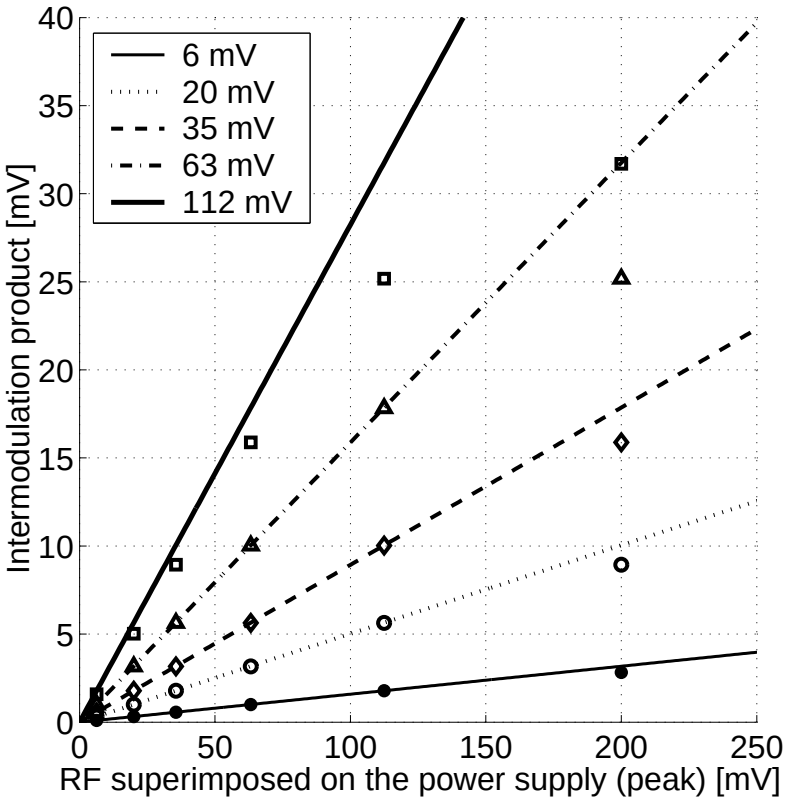


Figure 3.21. Amplitude of the intermodulation product (200kHz) versus the amplitude of the CW (200.2MHz) RF signal superimposed on the opamp power supply voltage is plotted for different values of the amplitude of the CW (200MHz) RF signal superimposed on the opamp input terminal (Folded Cascode Operational Amplifier connected voltage follower configuration). Points refer to experimental results while lines refer to model predictions

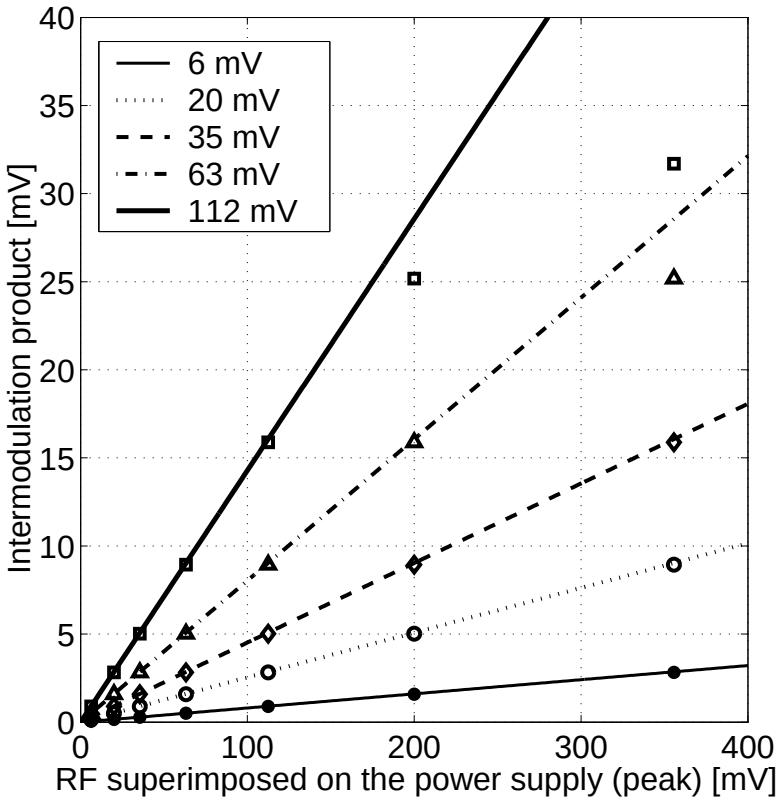


Figure 3.22. Amplitude of the intermodulation product (200kHz) versus the amplitude of the CW (500.2MHz) RF signal superimposed on the opamp power supply voltage is plotted for different values of the amplitude of the CW (500MHz) RF signal superimposed on the opamp input terminal (Folded Cascode Operational Amplifier connected in the voltage follower configuration). Points refer to experimental results while lines refer to model predictions

3.3.5 Conclusions

The effect of RF interference superimposed simultaneously on the input nominal signals and on the power supply voltage of opamps has been investigated and a new nonlinear model of CMOS feedback opamps has been presented. Such a model is based on a complete second order, three-input Volterra series representation of the nonlinear operation of the opamp input differential pair.

The proposed model grants a relationship among circuit parameters, parasitic elements and the intermodulation products, which are induced on the opamp output voltage by RF interference. As a consequence, such a model enable the designer to increase the immunity of opamp circuits to EMI.

The model predictions have been compared with the results of measurements carried on a folded cascode opamp connected in the voltage follower configuration which has been designed and fabricated by a 1μm standard BiCMOS technology process. A good agreement between experimental results and model predictions has been observed.

3.4 Closed-Form Large-Signal Model of RFI-Induced Distortion in CMOS Opamps

Even though the Volterra series opamp models which have been presented above can be very useful to IC designers in order to relate the susceptibility of opamp circuits to design parameters and parasitic elements, both these models suffer of intrinsic limitations when high amplitude RF interference is considered. In particular, as it has been observed above, Volterra series models are based on a polynomial approximation of the nonlinear characteristics of active devices therefore they do not capture properly the switching behavior of MOS transistors. When the amplitude of RFI is high enough to excite such switching behavior, i.e., it is high enough to turn off the opamp input devices, the accuracy of Volterra series models is very poor, even if higher order Volterra kernels would be included.

In present day low-voltage and very low voltage analog integrated circuits, however, the amplitude of RFI is very often comparable or even higher than the amplitude of nominal signals, therefore, the switching effects which have been described above should be considered in an RFI-oriented opamp model. In order to highlight these effects, a new modelling approach is required.

In recent years, a new operational amplifier nonlinear model that is suitable to the prediction of the RFI-induced offset voltage in linear feedback opamp circuits subjected to arbitrary amplitude RFI has been presented by Fiori [20]. This model provides a very good description of the nonlinear behavior of opamp circuits subjected to EMI and its predictions are in very good agreement with experimental data but it does not provide a closed form expression of RFI-induced offset voltage and the results which are provided are valid only under high-frequency RFI excitation.

In the following, after the results obtained by Fiori in [20] are summarized, a frequency dependent description of the RFI propagation within an opamp circuit is presented and a new MOS transistor model which captures the switching effects of MOS transistors under large signal RFI excitation is proposed. On the basis of these tools, the approach which has been adopted in [20] is employed and a frequency-dependent closed-form expression of the RFI induced offset in opamp circuits is derived. Finally, the prediction which have been obtained by the closed-form expression which has been presented are compared with the results of experimental tests which have been carried out by on wafer direct injection CW RFI measurements on three different opamp circuits which have been designed to this purpose with reference to the smart power BCD3s technology [35].

The information which is obtained from this model will be exploited in the next Chapter in the derivation design criteria which are suitable to enhance the susceptibility to EMI of opamp circuits.

3.4.1 Previous Results

In this Section, the results which have been obtained by Fiori in [20] and which will be employed in the following are presented.

In order to derive the new large-signal opamp model in [20], the nonlinear behavior of the opamp input differential pair has been taken into account, while the other opamp stages have been assumed to be linear. Therefore, the CMOS opamp circuit in Fig.3.23, which includes a differential pair that feeds a linear transimpedance amplifier has been referred to.

With reference to this model, the differential pair M1-M2 is made up of two source-coupled MOS transistors which are considered to be perfectly matched and at the same temperature. The gate terminals of M1 and M2 are driven by the input voltages $v^+(t)$ and $v^-(t)$ while their source terminals are biased by transistor M3 which acts as a current source I_B.

The differential current

$$i_\mathrm{D}(t) = i_{\mathrm{D1}}(t) - i_{\mathrm{D2}}(t)$$

drives the input of the transimpedance amplifier $Z_\mathrm{S}(\omega)$ which provides the opamp output voltage $v_0(t)$. The transimpedance $Z_\mathrm{S}(\omega)$ is assumed to be very high (ideally

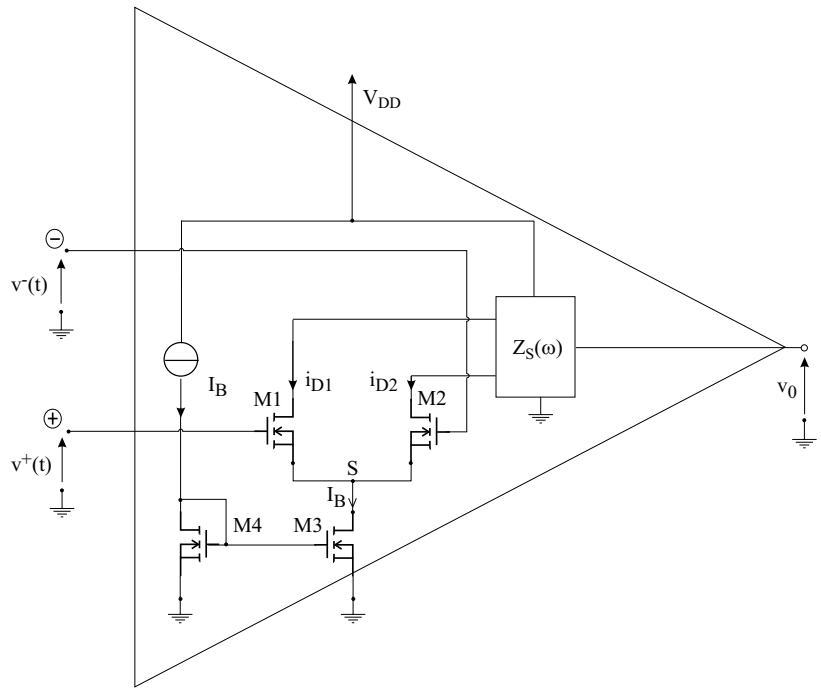


Figure 3.23. RFI-oriented opamp model.

infinite) within the opamp bandwidth, while it is assumed to be very low (ideally zero) out of the opamp bandwidth.

On the basis of the opamp macromodel in Fig.3.23, the RFI-induced offset in opamp circuits can be obtained by the approach proposed in [20]. This approach, which can be adopted for a general negative feedback opamp circuit, is now illustrated with reference to the voltage follower opamp circuit in Fig.3.24 to fix the ideas.

According with [20], the generation of the RFI induced offset can be regarded as follows: as the DC transimpedance $Z_S(0)$ is very high (ideally infinite), the mean value of the differential current $\bar{i}_D$ is strongly amplified by the transimpedance network. As the output voltage is fed back to the opamp inverting input, the consequent change in the opamp output voltage tends to compensate the mean value of the differential current which has induced it. In other words, the mean value of the differential current is kept very small (ideally zero) by a high-gain negative feedback loop, therefore

$$\bar{i}_{D1} = \bar{i}_{D2}. \tag{3.88}$$

On the contrary, the propagation of RFI is not affected by negative feedback. In fact, since the RF component of the differential current is blocked by the transimpedance amplifier $Z_S(\omega)$ and the RF component of the opamp output voltage is negligible. As the RFI which is superimposed onto the gate-to-source voltages of M1 and M2 induces changes in the mean value of the drain currents, the RFI-induced input offset voltage can be regarded as the DC voltage which is provided by the feedback to compensate the effects of distortion in order to keep to zero the mean value of the differential current.

On the basis of this reasoning, the RFI induced input offset voltage can be evaluated equating the mean values of the drain currents of M1 and M2 in the presence of RFI superimposed onto v_{GS1} and v_{GS2}, then solving this equation for the DC differential voltage which is provided by the feedback network. This evaluation has been performed numerically in [20], employing an expression of RFI superimposed onto v_{GS1} and v_{GS2} which has been evaluated under a high-frequency RFI assumption. In the following, a new model of the MOS transistor nonlinear operation will be presented which provides a closed-form expression of the RFI induced offset. Furthermore, the dependency on frequency of RFI superimposed onto v_{GS1} and v_{GS2} will be also considered.

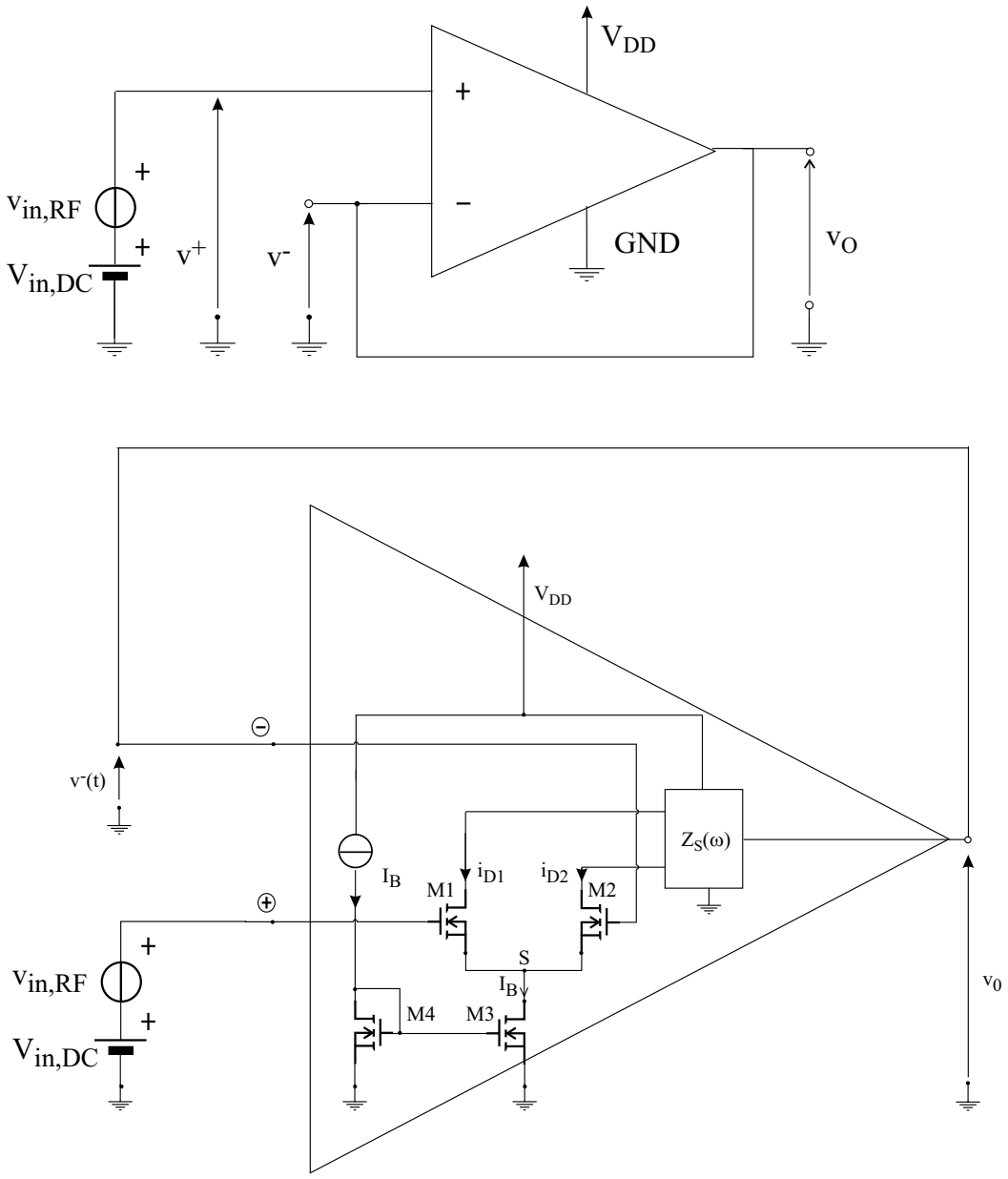


Figure 3.24. Voltage Follower Opamp circuit.

3.4.2 RFI Propagation in MOS Differential Pairs

In order to overcome the high frequency limitation of the approach proposed in [20], a frequency-dependent expression of the RF CW signals which excite the gate-to-source voltages of the input transistors of the differential pair in Fig. 3.23 is required.

This expression, which should be rigourously derived by frequency-domain large signal analysis, in practice can be effectively and accurately obtained from a small-signal linear circuit analysis in the frequency domain. In fact, due to their bandwidth limitations, CMOS opamps can be regarded as passive devices at RF and only their linear parasitic elements play a significative (typically filtering) role in the propagation of RFI. Furthermore, for the same reason, the high-frequency RFI which might be generated by the high-order distortion of active devices does not propagate through a CMOS opamp and therefore does not affect its operation.

With reference to the general passive negative feedback opamp circuit in Fig.3.25, the CW RFI which is superimposed onto the opamp inverting and non-inverting input voltages (v^- and v^+) can be expressed in the frequency domain in terms of the RF signals which are superimposed onto the input voltages of the overall circuit v_{IN1} and v_{IN2}. Such an analysis has been already detailed with reference to Volterra series models in previous Sections and it is not be repeated in the following where the frequency domain expressions $V^+_{\mathrm{RF}}(\omega)$ and $V^-_{\mathrm{RF}}(\omega)$ of the CW RF voltages that are superimposed onto the opamp input voltages are assumed to be known.

On the basis of $V^+_{\mathrm{RF}}(\omega)$ and $V^-_{\mathrm{RF}}(\omega)$, the frequency domain expression of the CW RFI that is superimposed onto the gate-to-source voltages of transistors M1 and M2 in Fig.3.23 can be derived with reference to the small signal equivalent circuit of the differential pair in Fig.3.26, which include all the parasitic capacitances of transistors M1, M2 and M3.

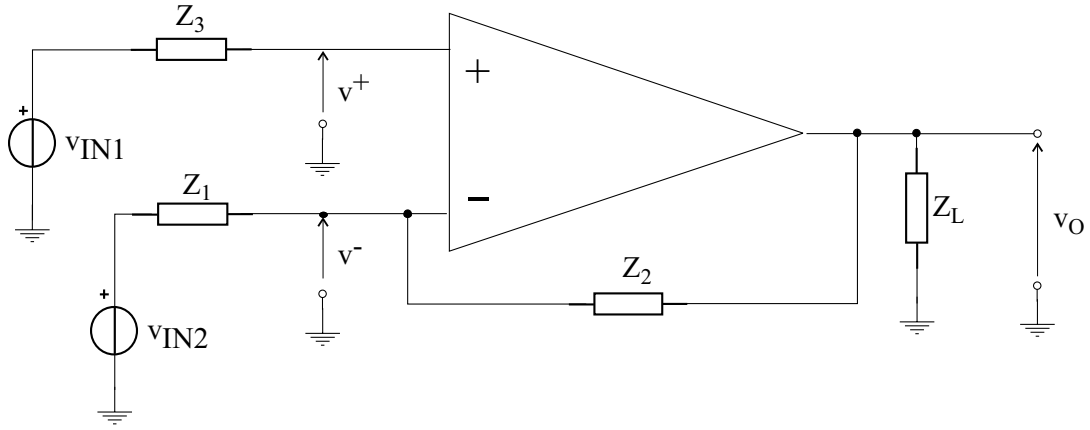
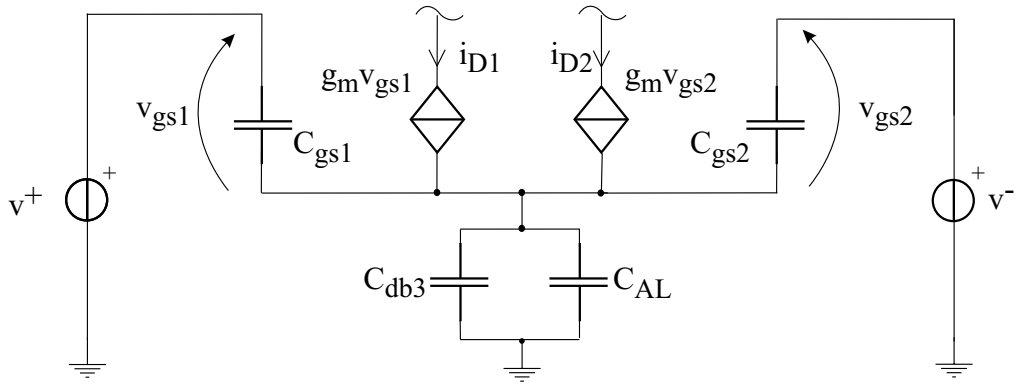
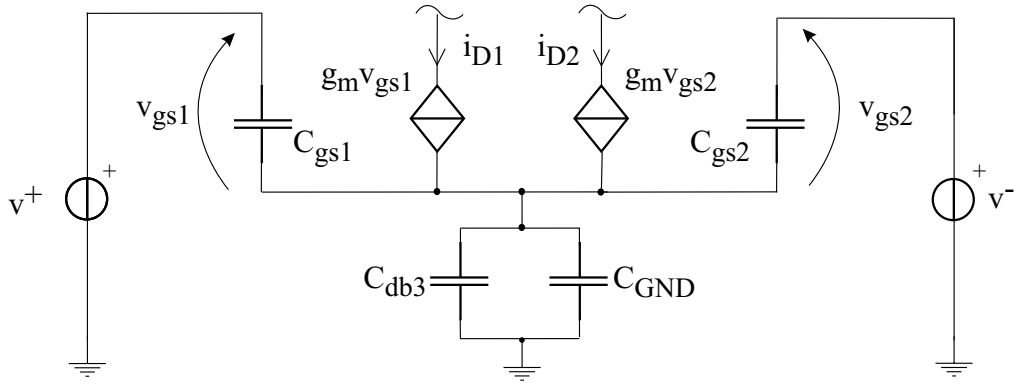


Figure 3.25. Linear Feedback Opamp Circuit.



a)



b)

Figure 3.26. Small-signal equivalent circuit of CMOS differential pairs with parasitic capacitances. a) nMOS differential pair b) pMOS differential pair.

In particular, from the frequency domain analysis of the circuit in Fig.3.4, the CW RF disturbances which are superimposed onto the gate-to-source voltages of transistors M1 and M2 can be written as follows

$$\begin{array}{rcrcrcr} V_{\mathrm{gs1,RF}}(\omega) & = & \alpha_1(\omega) & V^{+}_{\mathrm{RF}}(\omega) & + & (1-\alpha_2(\omega)) & V^{-}_{\mathrm{RF}}(\omega) \\ V_{\mathrm{gs2,RF}}(\omega) & = & (1-\alpha_1(\omega)) & V^{+}_{\mathrm{RF}}(\omega) & + & \alpha_2(\omega) & V^{-}_{\mathrm{RF}}(\omega) \end{array} \tag{3.89}$$

in which

$$\alpha_i(\omega) = \frac{g_{\mathrm{m}} + j\omega\,(C + C_{\mathrm{gs}i})}{2g_{\mathrm{m}} + j\omega\,(C + C_{\mathrm{gs1}} + C_{\mathrm{gs2}})} \qquad i = 1{,}2 \tag{3.90}$$

where g_{m} is the small-signal transconductance of M1 and M2 and

$$\begin{array}{ll} C = C_{\mathrm{db3}} + C_{\mathrm{AL}} & \text{in nMOS differential pairs} \\ C = C_{\mathrm{db3}} + C_{\mathrm{GND}} & \text{in pMOS differential pairs.} \end{array}$$

It can be observed from Eqn. (3.90) that

$$C_{\mathrm{gs1}} = C_{\mathrm{gs2}} = C_{\mathrm{gs}} \quad \Longrightarrow \quad \alpha_1(\omega) = \alpha_2(\omega) = \alpha(\omega).$$

Expressions (3.89) provide the effective amplitude of RFI superimposed onto the gate-to-source voltages of the input devices as a function of frequency. The effect of the nonlinearities in the propagation of RFI can be taken into account in (3.90) replacing small-signal parameters g_{m},C_{gs} and C in (3.90) with the corresponding amplitude dependent large-signal parameters $\widetilde{g}_{\mathrm{m}}$,$\widetilde{C}_{\mathrm{gs}}$ and $\widetilde{C}$, according with the approach which is presented in [21]. However, as it can be observed in Fig.3.27 where the ratio of large signal parameters and small signal parameter is plotted versus the peak amplitude of CW RF signals superimposed onto the nominal signal is presented, the impact of such a correction on the accuracy of the analysis is very small and it will not be employed in the following. The details of the large signal analysis which has been employed in order to derive the results plotted in Fig.3.27 have been reported in Appendix 3A.

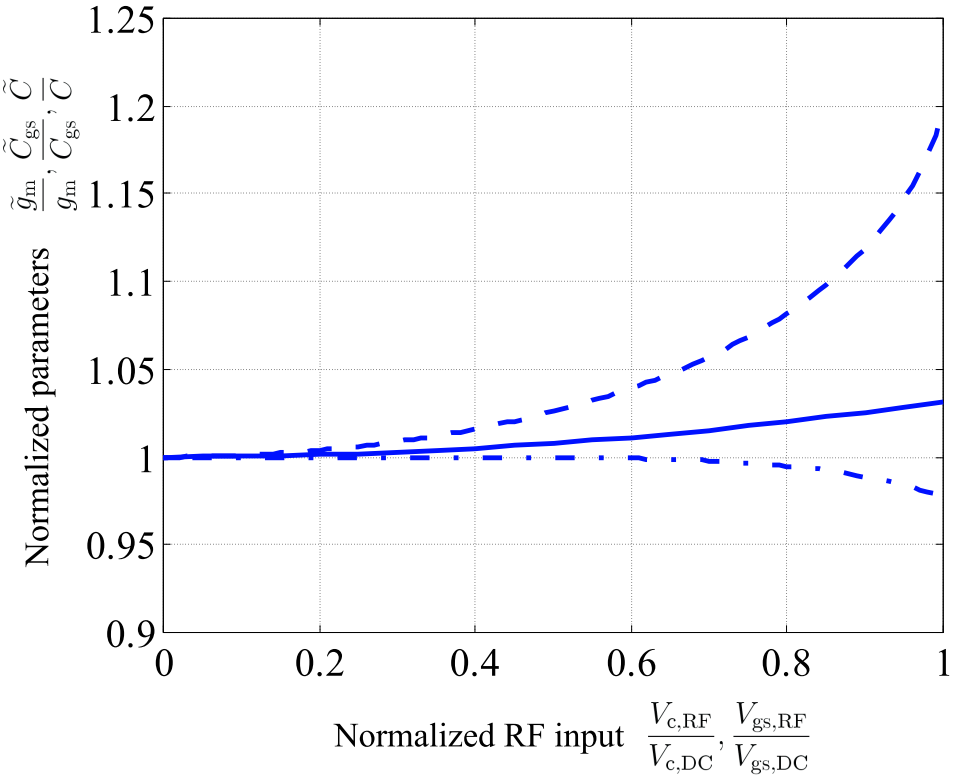


Figure 3.27. Large signal parameters normalized with respect to the corresponding small signal parameter $\frac{\widetilde{g}_{\mathrm{m}}}{g_{\mathrm{m}}}$, continuous line, $\frac{\widetilde{C}_{\mathrm{gs}}}{C_{\mathrm{gs}}}$, dot-dashed and $\frac{\widetilde{C}}{C}$, dashed versus RF input peak amplitude normalized with respect to the DC input $\left(\frac{V_{\mathrm{gs,RF}}}{V_{\mathrm{GS,DC}}}, \frac{V_{\mathrm{c,RF}}}{V_{\mathrm{C,DC}}}\right)$.

If

$$\omega > \frac{g_{\mathrm{m}}}{C + C_{\mathrm{gs1}} + C_{\mathrm{gs2}}},$$

then

$$\alpha(\omega) = \alpha = \frac{C + C_{\mathrm{gs}}}{C + 2C_{\mathrm{gs}}} = \frac{\frac{C}{C_{\mathrm{gs}}} + 1}{\frac{C}{C_{\mathrm{gs}}} + 2},$$

i.e. α is a real, frequency independent quantity that is only determined by the ratio of the parasitic capacitances of the differential pair. Finally, it can be observed that

$$\lim_{\frac{C}{C_{\mathrm{gs}}} \to 0} \alpha = \lim_{\frac{C}{C_{\mathrm{gs}}} \to 0} \alpha_i(\omega) = \frac{1}{2} \tag{3.91}$$

independently of frequency.

The above considerations on $\alpha_i(\omega)$ will be employed in the following to provide information on the role played by the parasitic capacitances of the differential pair in the susceptibility to RFI of opamp circuits.

3.4.3 Exponential MOS Transistor Model

In order to derive a closed-form expression of the RFI-induced offset shift in CMOS opamps on the basis of the approach proposed in [20], a new analysis-oriented model of MOS transistors working in the subthreshold and in the saturation region is proposed.

In particular, with reference to Fig.3.28, it is assumed that drain current i_{D} can be written in terms of the gate-to-source voltage v_{GS} as

$$\begin{aligned} i_{\mathrm{D}} &= I_{\mathrm{D0}}\, \mathrm{e}^{\frac{v_{\mathrm{GS}}}{V_{\mathrm{F}}}} \quad \text{for nMOS transistors} \\ i_{\mathrm{D}} &= I_{\mathrm{D0}}\, \mathrm{e}^{-\frac{v_{\mathrm{GS}}}{V_{\mathrm{F}}}} \quad \text{for pMOS transistors} \end{aligned} \tag{3.92}$$

where I_{D0} and V_{F} are model parameters which can be determined with reference to the nominal DC bias point (V_{GS},I_{D}) and to the small-signal transconductance g_{m} of the MOS transistors in the differential pair imposing

$$\begin{cases} i_{\mathrm{D}}\big|_{v_{\mathrm{GS}}=V_{\mathrm{GS}}} &= I_{\mathrm{D}} \\ \left.\frac{\partial i_{\mathrm{D}}}{\partial v_{\mathrm{GS}}}\right|_{v_{\mathrm{GS}}=V_{\mathrm{GS}}} &= g_{\mathrm{m}}. \end{cases} \tag{3.93}$$

On the basis of Eqn.(3.92), I_{D0} and V_{F} for a nMOS transistor can be expressed in terms of V_{GS}, I_{D} and g_{m} as

$$\begin{cases} V_{\mathrm{F}} &= \frac{I_{\mathrm{D}}}{g_{\mathrm{m}}} \\ I_{\mathrm{D0}} &= I_{\mathrm{D}}\, \mathrm{e}^{-\frac{g_{\mathrm{m}} V_{\mathrm{GS}}}{I_{\mathrm{D}}}}. \end{cases} \tag{3.94}$$

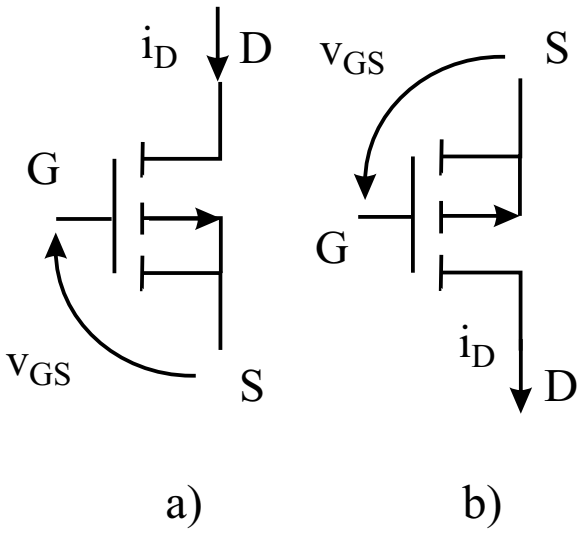


Figure 3.28. MOS Transistors.

The DC bias point (V_{GS},I_D) and the small-signal transconductance g_m can be expressed in terms of technology and design parameters by a physic-based MOS transistor model. In particular, on the basis of the physic-based model for an nMOS transistor in the saturation region

$$i_D = \beta \left(v_{GS} - V_T\right)^2, \tag{3.95}$$

in which

$$\beta = \frac{\mu_n C_{ox}}{2} \frac{W}{L}$$

where μ_n is the mobility of electrons in nMOS devices, C_{ox} is the capacitance of the gate oxide per unit of area and W and L are respectively the width and the length of the gate area of the MOS devices of the pair and V_T is the threshold voltage, the small signal transconductance can be expressed as

$$g_m = 2\sqrt{\beta I_D},$$

therefore Eqn.(3.94) can be written as

$$\begin{cases} V_F &= \frac{1}{2}\sqrt{\frac{I_D}{\beta}} \\ I_{D0} &= I_D \, e^{-2\left(1+V_T\sqrt{\frac{\beta}{I_D}}\right)}. \end{cases} \tag{3.96}$$

Furthermore, if an experimental DC characterization of an MOS transistor is available, I_{D0} and V_F can be determined in order to achieve the best fit of the model of Eqn.(3.92) with the experimental DC characteristic of the MOS transistors.

The model of the MOS transistor which has been presented in (3.92) is employed in the following for the evaluation of the RFI induced offset in CMOS opamps.

3.4.4 Offset Voltage Evaluation

On the basis of the MOS transistor model which has been presented in Eqn.(3.92), a closed-form expression of the RFI induced offset voltage in a CMOS opamp can be evaluated with the approach which has been presented in [20] and which has been summarized in Section 3.4.1.

On the basis of this reasoning, the RFI induced input offset voltage can be evaluated equating the mean values of the drain currents of M1 and M2 in the presence of RFI superimposed onto v_{GS1} and v_{GS2}, then solving this equation for the DC differential voltage which is provided by the feedback network. If the $i_{\mathrm{D}}(v_{\mathrm{GS}})$ expression in Eqn.(3.92) is employed and the gate-to-source voltages of M1 and M2 are written as

$$\begin{aligned} v_{\mathrm{GS1}}(t) &= V_{\mathrm{GS1,DC}} + |V_{\mathrm{gs1,RF}}| \cos(\omega t) \\ v_{\mathrm{GS2}}(t) &= V_{\mathrm{GS2,DC}} + |V_{\mathrm{gs2,RF}}| \cos(\omega t + \varphi) \end{aligned} \tag{3.97}$$

where $V_{\mathrm{GS}i\mathrm{,DC}}$ are the DC values of the gate-to-source voltages, $|V_{\mathrm{gs}i\mathrm{,RF}}|$ are the peak amplitudes of the CW RFI which have been derived in (3.89) and, again from (3.89),

$$\varphi = \angle V_{\mathrm{gs2,RF}} - \angle V_{\mathrm{gs1,RF}},$$

Eqn.(3.88) takes the form

$$\frac{1}{T}\int_0^T I_{\mathrm{D0}} \mathrm{e}^{\frac{V_{\mathrm{GS1,DC}} + \left|V_{\mathrm{gs1,RF}}\right| \cos \omega t}{V_{\mathrm{F}}}} \mathrm{d}t = \frac{1}{T}\int_0^T I_{\mathrm{D0}} \mathrm{e}^{\frac{V_{\mathrm{GS2,DC}} + \left|V_{\mathrm{gs2,RF}}\right| \cos(\omega t + \varphi)}{V_{\mathrm{F}}}} \mathrm{d}t \tag{3.98}$$

where $T = \frac{2\pi}{\omega}$. Solving the integrals, Eqn.(3.98) becomes

$$\mathrm{e}^{\frac{V_{\mathrm{GS1,DC}}}{V_{\mathrm{F}}}} I_0\left(\frac{|V_{\mathrm{gs1,RF}}|}{V_{\mathrm{F}}}\right) = \mathrm{e}^{\frac{V_{\mathrm{GS2,DC}}}{V_{\mathrm{F}}}} I_0\left(\frac{|V_{\mathrm{gs2,RF}}|}{V_{\mathrm{F}}}\right) \tag{3.99}$$

where $I_n(x)$ is the modified Bessel function of the first kind of order n.

From Eqn.(3.99), through elementary algebraic manipulations, the RFI induced DC offset voltage $\Delta V_{\mathrm{off}} = V_{\mathrm{GS1,DC}} - V_{\mathrm{GS2,DC}}$ can be expressed as

$$\Delta V_{\mathrm{off}} = V_{\mathrm{F}} \ln \frac{I_0\left(\frac{\left|V_{\mathrm{gs2,RF}}\right|}{V_{\mathrm{F}}}\right)}{I_0\left(\frac{\left|V_{\mathrm{gs1,RF}}\right|}{V_{\mathrm{F}}}\right)} \tag{3.100}$$

Eqn.(3.100) provides a very compact expression for the RFI-induced offset voltage in a CMOS opamp and can be employed both to predict the susceptibility to RFI of a given opamp circuit and to relate this susceptibility to design parameters and parasitics.

3.4.5 Model Validation

The large signal analytical model for the prediction of EMI induced distortion in feedback opamp circuits which has been presented above will be validated by comparison of model prediction and experimental results which have been obtained with reference to three different widely employed opamp circuit topologies.

Devices Under Test

In order to validate the new model, three opamp circuits have been considered: an nMOS-Input Miller opamp, a pMOS-Input Miller opamp and an nMOS-input Folded Cascode opamp. The schematic views of these three circuits are reported in Fig.3.29, Fig.3.30 and Fig.3.31 respectively while their main electrical parameters are shown in Table 3.3. All these circuits have been connected in the voltage follower configuration, as shown in Fig.3.24 and have been integrated on silicon in the 1μm technology process BCD3s [35]. In Fig.3.32 a die photo of the pMOS-Input Miller opamp is provided.

The parameters which have been employed in the models to obtain a prediction of the RFI induced offset voltage have been obtained from the data of the technology process BCD3s on which the circuits have been developed.

Table 3.3. Electrical Characteristics of the opamp circuits employed for model validation

Parameter	Unit	circuit #1	circuit #2	circuit #3
Opamp Topology		Miller	Miller	Fold. Casc.
Input Differential Pair		nMOS	pMOS	nMOS
Opamp Circuit		Volt. Foll.	Volt. Foll.	Volt. Foll.
Power Supply, V_{DD}	V	5	5	5
Differential Gain, A_d	dB	84	74	88
Phase Margin	degrees	90	90	90
CMRR	dB	100	100	120
PSRR	dB	95	90	110
Slew Rate	V/μs	3	3	3
Output Current	μA	200	200	400
Gain-Bandwidth	MHz	2.8	4	5

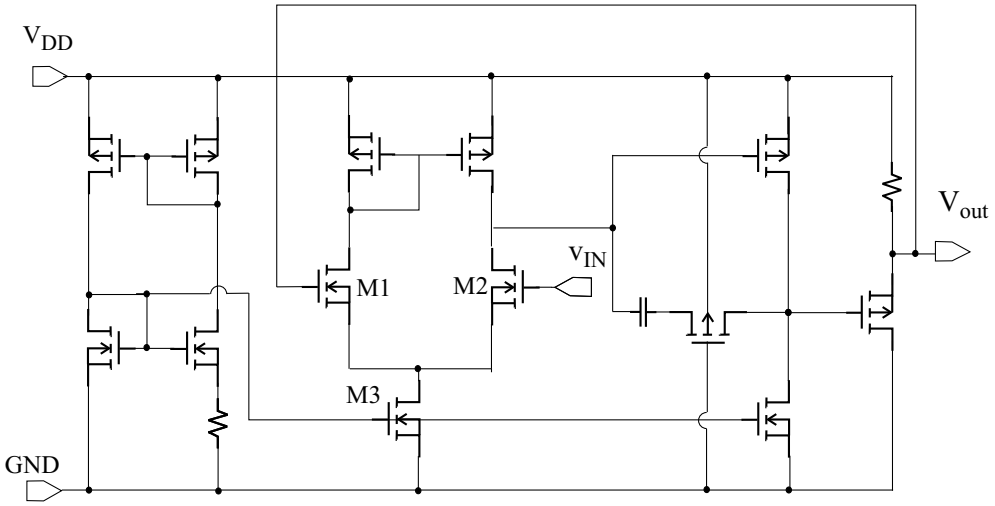


Figure 3.29. nMOS-Input Miller Opamp Schematic.

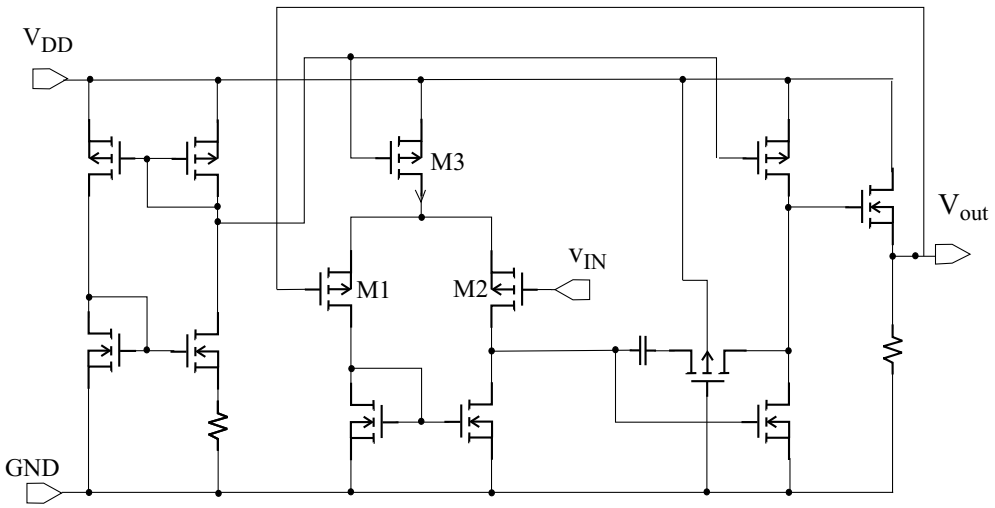


Figure 3.30. pMOS-Input Miller Opamp Schematic.

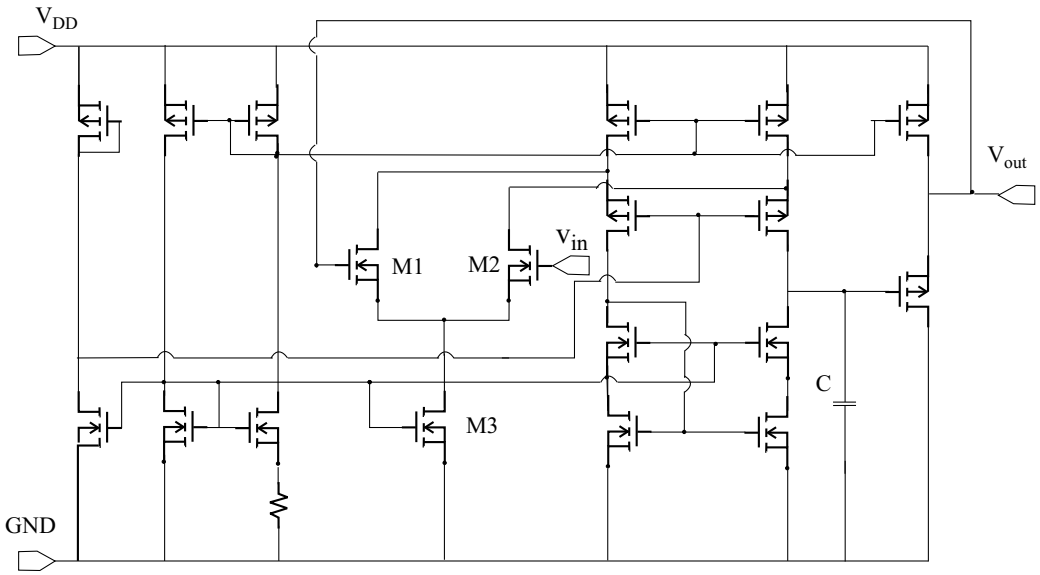


Figure 3.31. nMOS-Input Folded Cascode Opamp Schematic.

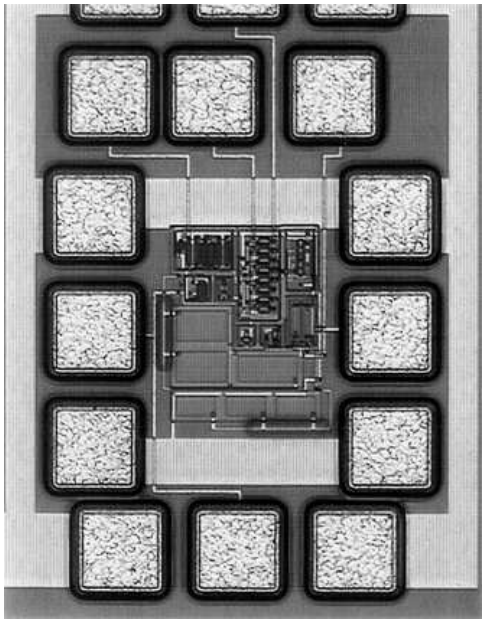


Figure 3.32. pMOS-Input Miller Opamp Die Photo.

Measurement Test Setup

The test bench shown in Fig.3.12 has been employed to carry out the on-chip measurements which are required for the validation of the new model. In this bench, a wafer probe station [36] is employed and the input *ground-signal-ground* (GSG) pads of the voltage follower opamp circuit are contacted by an RF probe [37], which is connected to a bias tee: the DC input of the bias tee is connected to a DC voltage source $V_{\mathrm{IN,DC}}$ [38], while its RF input is connected to an RF source [39] in order to superimpose RF signals on the nominal DC input voltage of the opamp.

The output GSG pads of the opamp are contacted by an RF probe, which is connected to a bias tee as well: its DC port is connected to a DC voltmeter [40] in order to measure the DC component of the output voltage while the RF port is connected to a load $R_{\mathrm{L}} = 50\Omega$. Finally, the DC power supply voltage for the amplifier is provided by a 5V DC voltage source V_{dd} [38].

In order to measure the RFI-induced DC offset voltage shift, the DC output voltages, which have been measured with and without RF interference added to the DC input voltage V_{IN}, have been compared for all the devices under test.

Experimental Results

In Fig.3.33, Fig.3.34 and Fig.3.35 the predicted (continuous line) and measured (circles) RFI induced offset voltage in the nMOS-Input Miller opamp, in the pMOS-Input Miller opamp and in the nMOS-input Folded Cascode opamp respectively are plotted versus the peak amplitude $V_{\mathrm{in,RF}}$ of the CW (100MHz) RFI superimposed onto the voltage follower input terminal.

From these plots, it can be observed that the predictions which are provided by the new model are very accurate even under large signal RFI excitation. In particular, from Fig.3.36 and Fig.3.37, in which the relative and the absolute error in the prediction of the RFI induced offset voltage are plotted with reference to the nMOS-Input Miller opamp, it can be observed that the relative error is always below 3% while the absolute error is below 6mV.

In Fig.3.38 the predicted (continuous line) and measured (diamonds) RFI induced offset voltage in the CMOS-Input Miller opamp is plotted versus the frequency of a CW RFI with a peak amplitude of 300mV. The error between model prediction and experimental results, which is larger than in the previous plots, can be ascribed to experimental inaccuracies in the calibration of the RF input power injected for different frequencies.

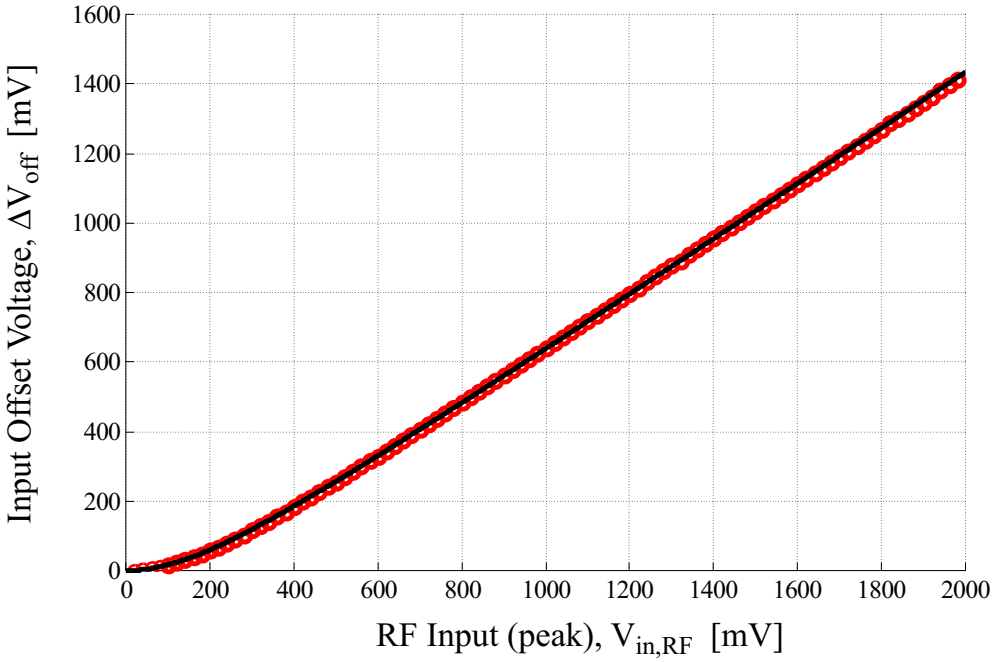


Figure 3.33. Predicted (continuous line) and measured (circles) RFI-induced Input Offset Voltage versus the peak amplitude $V_{\mathrm{in,RF}}$ of CW RFI in the nMOS Input Miller Opamp.

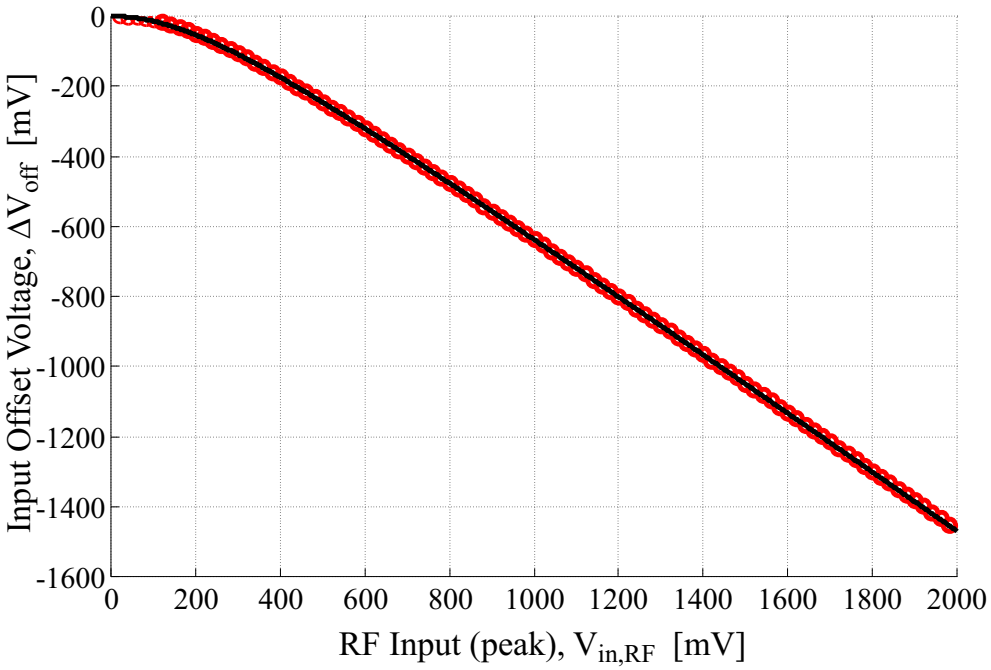


Figure 3.34. Predicted (continuous line) and measured (circles) RFI-induced Input Offset Voltage versus the peak amplitude $V_{\mathrm{in,RF}}$ of CW RFI in the pMOS Input Miller Opamp.

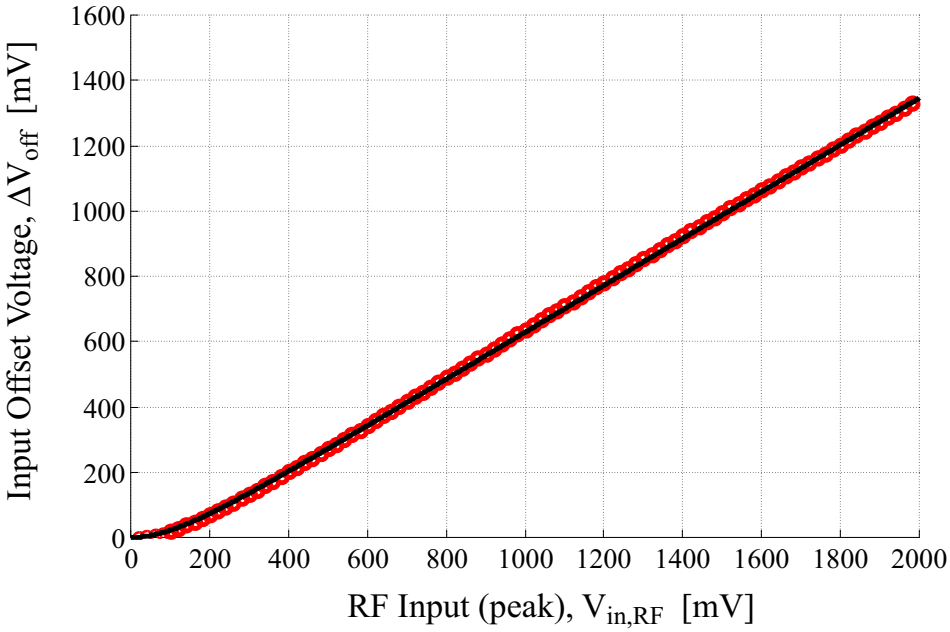


Figure 3.35. Predicted (continuous line) and measured (circles) RFI-induced Input Offset Voltage versus the peak amplitude $V_{\mathrm{in,RF}}$ of CW RFI in the nMOS Input Folded Cascode Opamp.

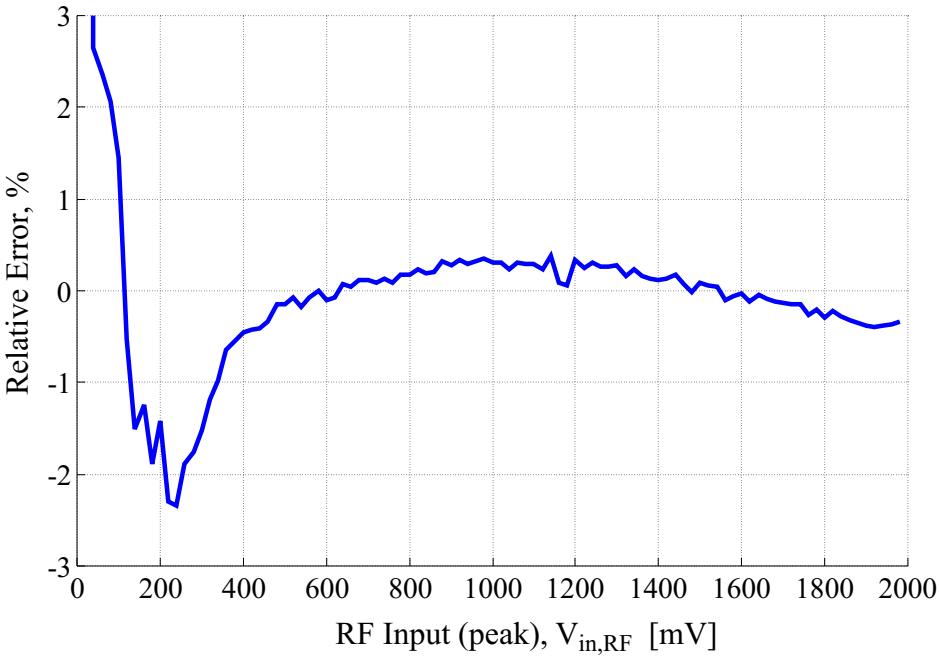


Figure 3.36. Model prediction relative error versus CW RFI peak amplitude with reference to the nMOS-Input Miller Opamp (cfr. Fig.3.33).

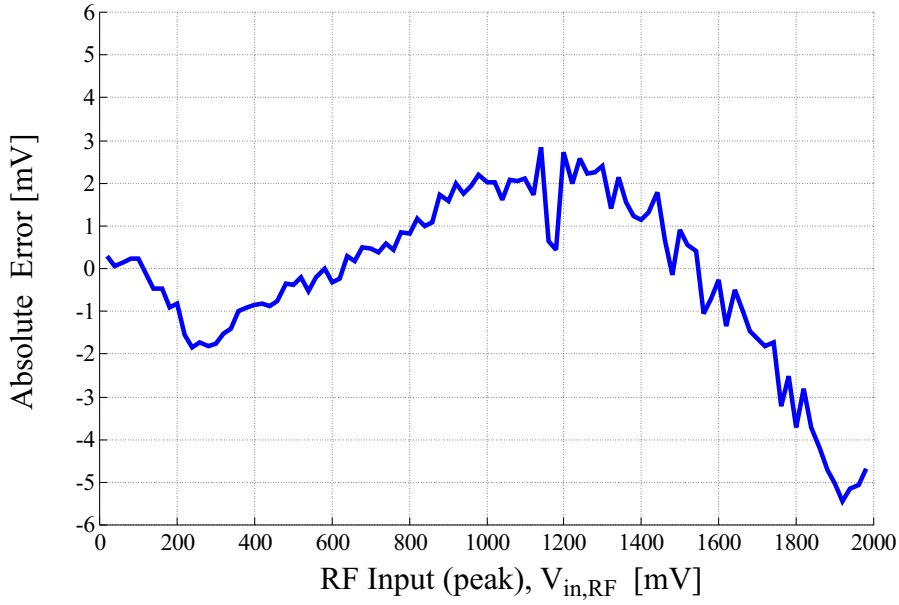


Figure 3.37. Model Prediction absolute error versus CW RFI peak amplitude with reference to the nMOS-Input Miller Opamp (cfr. Fig.3.33).

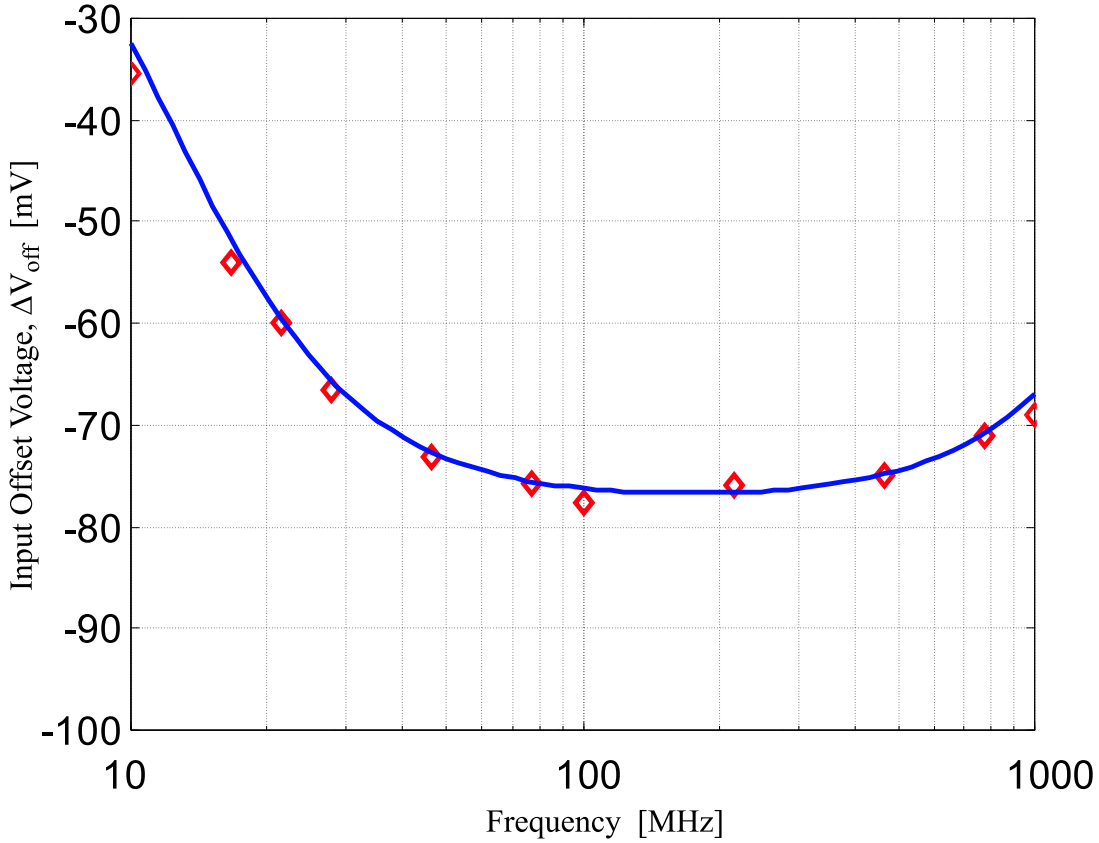


Figure 3.38. Predicted (continuous line) and measured (diamonds) RFI-induced Input Offset Voltage versus frequency of a CW RFI with a peak amplitude of 300mV in the pMOS Input Miller opamp.

3.4.6 Conclusion

The new closed-form expression which has been derived above on the basis of the numerical model which has been proposed by Fiori [20] provides a very accurate prediction of the RFI-induced offset voltage in CMOS opamp circuits.

The predictions of the new model have been compared with the results of experimental tests that have been carried out on three different CMOS opamp circuits. For each circuit, the prediction obtained by the new model are in very close agreement with the experimental results.

Such an expression can be useful both for the prediction of the susceptibility to RFI of a given opamp circuit and to the design of opamp circuits which are immune to RFI. To this purpose, in particular that expression will be employed in the next Chapter.

Appendix 3A

Consider a nonlinear circuit excited by a single RF signal with frequency ω_0 and peak amplitude V_0. If we are only interested in the component at frequency ω_0 of an output quantity and high-order high-frequency distortion signals are negligible and/or do not propagate throughout the circuit, such a circuit can be analyzed, according with the describing function method, as a linear circuit in which each transfer function depends on the amplitude of the input signal (fundamental component). In particular, each nonlinear circuit element can be formally regarded as a linear circuit element whose value depends on the amplitude of the input signal.

Under these assumptions, the nonlinearity in the propagation of RFI can be taken into account considering the large signal parameters $\widetilde{g}_{\rm m}$,$\widetilde{C}_{\rm gs}$ and $\widetilde{C}$ in (3.89) defined as follows:

$$\begin{aligned} \widetilde{g}_{\rm m}(V_{\rm GS,DC},V_{\rm gs,RF}) &= \frac{I_{\rm d,RF}}{V_{\rm gs,RF}} \qquad (3.101)\\ &= \frac{1}{V_{\rm gs,RF}}\frac{2}{T}\int_0^T i_{\rm D}(v_{\rm GS})|_{V_{\rm GS,DC}+V_{\rm gs,RF}\cos(\omega_0 t)}\cos(\omega_0 t){\rm d}t \end{aligned}$$

$$\begin{aligned} \widetilde{C}(V_{\rm C,DC},V_{\rm c,RF}) &= \frac{Q_{\rm c,RF}}{V_{\rm c,RF}} \qquad (3.102)\\ &= \frac{1}{V_{\rm c,RF}}\frac{2}{T}\int_0^T q_{\rm C}(v_{\rm C})|_{V_{\rm c,DC}+V_{\rm c,RF}\cos(\omega_0 t)}\cos(\omega_0 t){\rm d}t \end{aligned}$$

$$\begin{aligned} \widetilde{C}_{\rm gs}(V_{\rm GS,DC},V_{\rm gs,RF}) &= \frac{Q_{\rm gs,RF}}{V_{\rm gs,RF}} \qquad (3.103)\\ &= \frac{1}{V_{\rm gs,RF}}\frac{2}{T}\int_0^T q_{\rm GS}(v_{\rm GS})|_{V_{\rm GS,DC}+V_{\rm gs,RF}\cos(\omega_0 t)}\cos(\omega_0 t){\rm d}t \end{aligned}$$

A nonlinear static expression for $i_{\rm D}(v_{\rm GS})$ in Eqn. (3.101) is given in Eqn. (3.92), in Eqn.(3.102) the expression for the charge in an inverse-biased junction

$$q_{\rm C}(v_{\rm C}) = Q_0\sqrt{1+\frac{v_{\rm C}}{\phi}} \qquad (3.104)$$

where Q_0 and ϕ are technological parameters can be employed and in Eqn. (3.103) one can employ the expression for the gate charge in saturation and in subthreshold regions reported in [43]

$$q_{\mathrm{GS}}(v_{\mathrm{GS}}) = C_{\mathrm{gso}} v_{\mathrm{GS}} + (C_{\mathrm{gs,sat}} - C_{\mathrm{gso}}) \eta \log\left(1 + \mathrm{e}^{\frac{v_{\mathrm{GS}}}{\eta}}\right) \tag{3.105}$$

where C_{gso} is the gate-source overlap capacitance in subthreshold region, $C_{\mathrm{gs,sat}}$ is the gate-source capacitance for an MOS transistor in saturation due to the conductive channel and η is a parameter employed to achieve a smooth transition between these two values.

Employing the above mentioned nonlinear static expressions, in Fig.3.27 the large-signal parameters normalized with respect to the value of the corresponding small-signal parameters, $\frac{\widetilde{g}_{\mathrm{m}}}{g_{\mathrm{m}}}, \frac{\widetilde{C}_{\mathrm{gs}}}{C_{\mathrm{gs}}}$ and $\frac{\widetilde{C}}{C}$ are plotted as a function of the amplitude of the RF signal normalized with respect to the amplitude of the DC input signal $\left(\frac{V_{\mathrm{c,RF}}}{V_{\mathrm{C,DC}}}, \frac{V_{\mathrm{gs,RF}}}{V_{\mathrm{GS,DC}}}\right)$ for realistic values of the technology parameters and realistic bias conditions.

It can be observed from Fig.3.27 that the impact of the nonlinearity in the propagation of RFI is practically negligible, therefore it has not been considered in the derivation of the model presented above.

Chapter 4

EMI-Aware Operational Amplifier Circuit Design

The insight in the RFI-induced phenomena in opamp operation, which has been gained from the analytical models that have been discussed in the previous Chapter, is now translated into high-immunity operational amplifier design criteria.

Firstly, the susceptibility to EMI of negative feedback opamp configurations is related to the susceptibility of the opamp cell and the benchmarks which can be employed in order to compare the susceptibility of different opamp cells are discussed. To this purpose, the susceptibility to EMI of different negative feedback opamp configurations, which has been previously investigated in the literature [16, 17, 44] by experimental results and computer simulation, is revised on the basis of the analysis of the previous Chapter.

Then, the intrinsic susceptibility to RFI of an opamp cell is addressed. To this purpose, the influence of opamp design parameters and parasitic elements in the susceptibility to EMI of an IC opamp circuit is discussed by the comparison of the RFI-induced offset voltage in the voltage follower configuration on the basis of the analytical expression that has been derived in the previous Chapter.

Moreover, the tradeoffs in terms of performance, which should be considered in the design of standard opamp topologies in order to achieve a low susceptibility to EMI, are highlighted and the opamp design goals, which are in contrast or agree with a high immunity to EMI, are discussed.

Furthermore, a new high-immunity opamp input stage is presented and its operation principle is discussed. The immunity to EMI of this circuit, in particular, has been predicted on the basis of Volterra series analysis. This new opamp input stage has been included in a CMOS folded cascode opamp topology and its low susceptibility to EMI has been verified by time-domain computer simulations.

Finally, the effectiveness of the design criteria, which are presented in this work, in the design of analog integrated sub-systems robust to EMI is considered.

4.1 RFI in Feedback Opamp Circuits

The susceptibility of negative feedback opamp circuits to RFI superimposed onto the input voltages depends both on the nonlinear distortion characteristics of the opamp circuit itself and on the amplitude of RF signals superimposed onto the opamp nominal voltages. The latter, in particular depends on the amplitude of the RFI which is superimposed onto the external inputs of a feedback opamp circuit and on the linear feedback network configuration. As a consequence, the immunity of a negative feedback opamp circuit is addressed both reducing the amplitude of RFI superimposed onto the opamp input terminals by a proper sizing of the feedback network and addressing the intrinsic susceptibility of the opamp cell.

The effects of the feedback configuration on the susceptibility to EMI of opamp circuits have been already investigated in the literature on the basis of computer simulations and experiments in [16, 17, 44] where the filtering effect of feedback components and of their parasitics have been highlighted. In this work, the intrinsic susceptibility of the opamp circuits is addressed. Nonetheless, the effects of the feedback network will be firstly revised on the basis of the analysis which has been carried out in the previous Chapter in order to relate the susceptibility of negative feedback opamp circuits to the opamp cell susceptibility for the sake of comparison.

4.1.1 Input-Referred RFI-Induced Distortion

In order to compare the susceptibility to RFI of different negative feedback opamp circuits which process the input signal(s) in different ways, it is convenient to refer the opamp RFI-induced distortion to the opamp input voltage. To this purpose, the RFI-induced distortion in the differential pair differential current Δi_{D} can be divided by the differential pair transconductance g_{m}, according with the approach that has been presented in [32] or, alternatively, the large signal approach in the last Section of the previous Chapter can be employed.

Therefore, the opamp circuit which is shown in Fig.4.1a, in which RFI equivalent voltage sources v_{RF1} and v_{RF2} are included, is equivalent for in-band analysis to the circuit in Fig.4.1b, where the RFI-induced distortion of the opamp is taken into account by the voltage source

$$\Delta v_{\mathrm{LF}} = \frac{\Delta i_{\mathrm{D}}}{g_{\mathrm{m}}}.$$

In the presence of CW RFI, the input-referred low frequency distortion Δv_{LF} is a DC voltage, which is referred to as *RFI-induced Input Offset Voltage Shift*, ΔV_{off}. This parameter is particularly expressive for the sake of comparison of the effects of EMI on nominal opamp circuit operation.

In the previous Chapter it has been shown, with reference to a negative feedback opamp configuration, that ΔV_{off} depends both on the intrinsic susceptibility of the

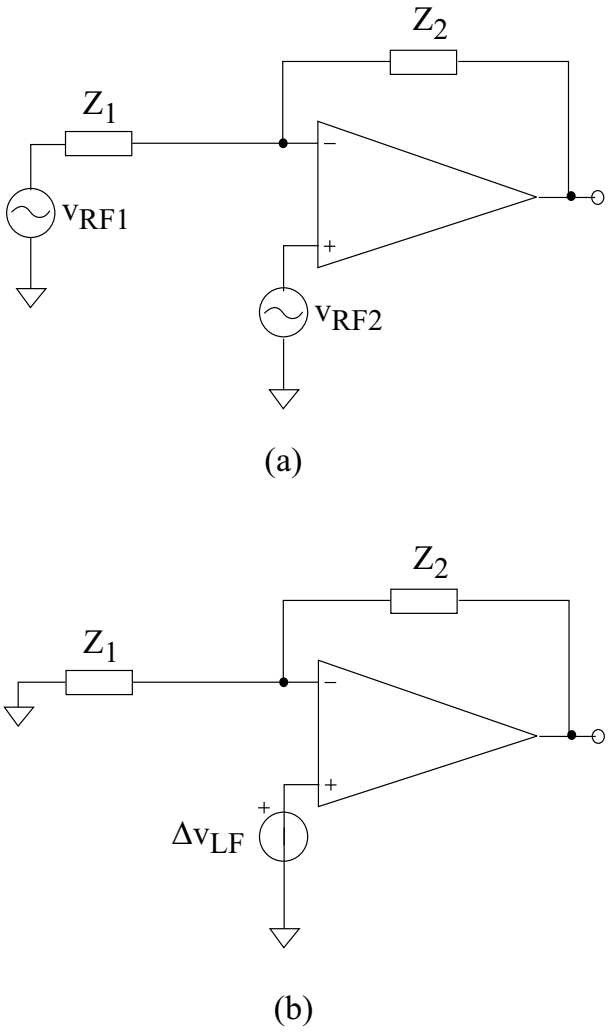


Figure 4.1. Input-Referred EMI-Induced Distortion in Feedback Opamp Circuits.

opamp circuit and on the amplitude of RFI superimposed onto the opamp input terminals. From the results of Volterra series analysis in Section 3.2.1, ΔV_{off} is related to the CW RFI superimposed onto the opamp input voltages and, in particular

$$\Delta V_{\text{off}} \propto |V_{\text{cm}}(\omega)|\,|V_{\text{d}}(\omega)| \tag{4.1}$$

where $|V_{\text{cm}}(\omega)|$ and $|V_{\text{d}}(\omega)|$ are the peak amplitudes of common mode and differential mode CW RFI superimposed onto the opamp input voltages.

Therefore, if either the differential or the common mode RFI superimposed onto the opamp input terminals is negligible, almost no RFI distortion is induced whereas if both common mode and differential mode RFI is simultaneously superimposed

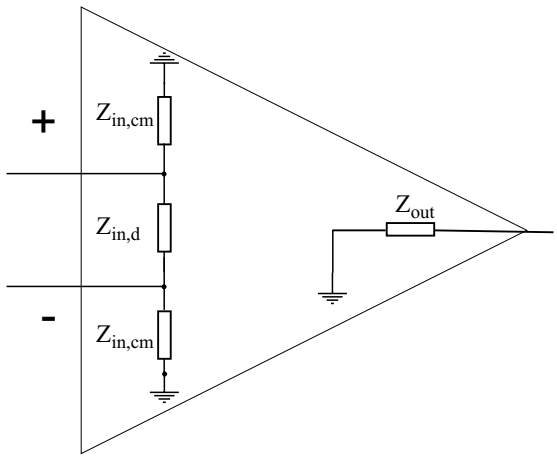


Figure 4.2. Opamp Linear Model for RFI Propagation Calculations

onto the opamp input voltages the amount of RFI induced distortion can be significative. Furthermore, the quantity

$$|V_{\mathrm{cm}}(\omega)|\,|V_{\mathrm{d}}(\omega)|\,, \tag{4.2}$$

which is only related to RFI propagation through the opamp feedback network, can be conveniently employed for the comparison of different opamp feedback configurations in terms of susceptibility to EMI. Conversely, for the sake of comparison, the intrinsic susceptibility to RFI of an opamp circuit should be considered for a given value of the product (4.2).

With reference to different feedback opamp topologies, RFI superimposed onto the differential and common mode opamp input voltages can be expressed in terms of RFI superimposed onto the external voltages by frequency domain linear analysis on the basis of the opamp linear model in Fig.4.2. The effectiveness of this approach in the analysis of RFI propagation has been discussed in the previous Chapter, in which the impact of nonlinearity in high-frequency RFI propagation has been shown to be negligible.

On the basis of this approach, the susceptibility to EMI of the basic opamp feedback configurations shown in Fig.4.3 (i.e. inverting, non-inverting and voltage follower configurations) can be compared.

4.1.2 Comparison of Feedback Opamp Configurations

With reference to the inverting opamp topology in Fig.4.3a, it can be observed that

$$V_{\rm d}(\omega) = -V^{-}(\omega) \qquad V_{\rm cm}(\omega) = \frac{V^{-}(\omega)}{2}, \tag{4.3}$$

where

$$V^{-}(\omega) = \frac{Z_2'}{Z_1 + Z_2'} V_{\rm EXT}(\omega) \tag{4.4}$$

in which

$$Z_2' = [Z_2 + (Z_{\rm L} \parallel Z_{\rm out})] \parallel (Z_{\rm in,d} + Z_{\rm in,cm}) \parallel Z_{\rm in,cm}$$

and, with reference to the non-inverting opamp topology in Fig.4.3b,

$$V_{\rm d}(\omega) = \frac{Z_{\rm in,d}}{Z' + Z_{\rm in,d}} V_{\rm EXT}(\omega) \qquad V_{\rm cm}(\omega) = \frac{2Z' + Z_{\rm in,d}}{2(Z' + Z_{\rm in,d})} V_{\rm EXT}(\omega), \tag{4.5}$$

where

$$Z' = Z_1 \parallel (Z_2 + Z_{\rm out} \parallel Z_L) \parallel Z_{\rm in,cm}.$$

In both inverting and non-inverting opamp circuits it can be observed that, assuming that all the impedances are RC impedances[1], which is usually the case in integrated circuits, differential and common mode RFI superimposed onto the opamp input voltages is attenuated by the feedback network and it is related to the external RFI input voltage $V_{\rm EXT}$ in a frequency dependent way.

The RFI filtering effect which has been highlighted above can be enhanced by design in order to reduce the susceptibility to RFI of these feedback configurations [16, 17, 44]. Nonetheless, these configurations are not suitable to the investigation of the intrinsic susceptibility of the opamp cells, which may be masked by the filtering effect of the feedback network.

In the voltage follower opamp circuit in Fig.4.3, instead, the opamp inverting input is connected to the AC reference voltage by a low impedance as

$$|Z'| = |(Z_{\rm in,cm} \parallel Z_{\rm L} \parallel Z_{\rm out})|,$$

is usually very low at RF, in particular if the voltage follower circuit is capacitively loaded. As a consequence, the differential and common mode RFI superimposed onto the opamp input voltages can be expressed as

$$V_{\rm d} = V_{\rm EXT}(\omega) \qquad V_{\rm cm} = \frac{V_{\rm EXT}(\omega)}{2}. \tag{4.6}$$

[1]If Z_1 and Z_2 are pure RC (or RL) impedances $|Z_1 + Z_2| \geq |Z_1|,|Z_2|$ and $|(Z_1 \parallel Z_2)| \leq |Z_1|,|Z_2|$. This property is not true, in general, for RLC impedances in which resonant phenomena might occur.

In particular, the common-mode and differential-mode RF components of the opamp input voltage are directly related to the CW RFI peak amplitude onto the voltage follower external input which is substantially not attenuated by the feedback network. Therefore, the voltage follower circuits is a worst-case condition in terms of susceptibility to EMI among the other opamp feedback configurations, in agreement with the experimental results provided by Masetti et al. in [16, 17]. Furthermore, the amplitude of differential and common mode signals which are superimposed onto the opamp input voltage are related to the RF input signal in a frequency independent way. These features make the voltage follower configuration suitable as a benchmark in order to compare the intrinsic susceptibility to RFI of different opamp circuits.

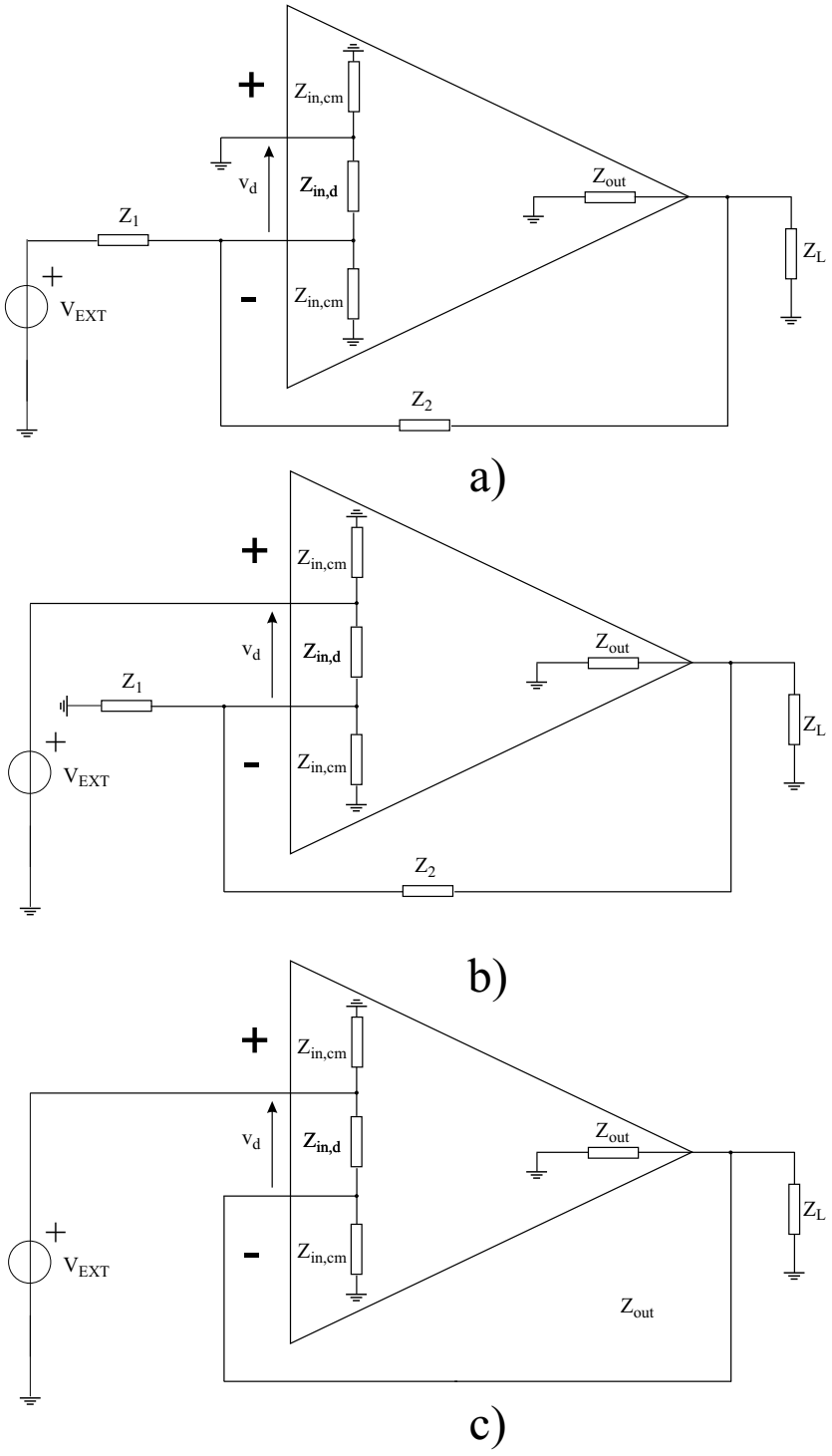


Figure 4.3. Inverting, Non-Inverting and Voltage Follower Feedback Opamp Circuits

4.2 High Immunity Opamp Design Criteria

In the previous Section, the influence of the feedback configuration on the susceptibility to EMI of opamp circuits has been revised and it has been observed that the feedback network provides a filtering effect on EMI. Such effect can be enhanced by a proper design of the feedback network in order to reduce the susceptibility to EMI of a given feedback opamp configuration. Nonetheless, the robustness to EMI of a given feedback opamp circuit would be enhanced more effectively if the opamp itself, which is included in it, is designed to be intrinsically immune to EMI, i.e. if it generates no in-band distortion even in the presence of differential and common mode RF signals superimposed onto its nominal input voltages. Any improvement at this level, in fact, improves the susceptibility of any opamp configuration independently on its feedback network.

In this Section the enhancement of the immunity to EMI of an opamp circuit by design is addressed. To this purpose, the intrinsic susceptibility to EMI of an opamp circuit versus CW RFI amplitude and frequency is firstly considered, then, the impact of design parameters on RFI distortion, are discussed on the basis of the opamp circuit models which have been presented in the previous Chapter. In particular, the large-signal model of RFI distortion will be considered, which describes accurately the behavior of opamp circuits even in the presence of large-signal RFI.

In order to investigate the susceptibility to EMI of an opamp circuit independently of the feedback configuration in which it is connected, the RFI-induced input offset voltage in the voltage follower opamp configuration shown in Fig.4.4 in which CW RFI signals are superimposed onto the external input terminal is considered as a benchmark. As it has been observed above, this configuration represents the worst case among negative feedback opamp circuits in terms of susceptibility to RFI.

Furthermore, for the sake of comparison, the default values in Tab.4.1 are considered for the parameters which are not specified in each analysis. The values of

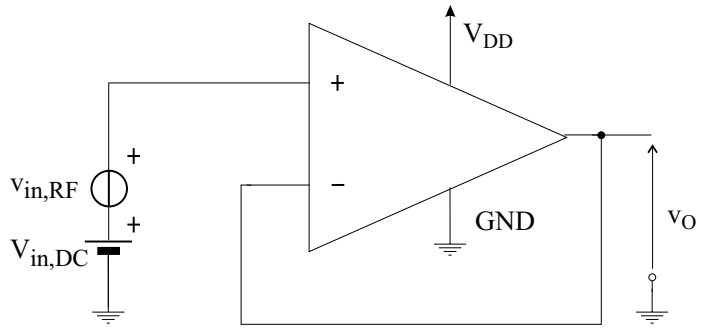


Figure 4.4. Voltage Follower Opamp Circuit as an EMI Susceptibility Benchmark

the technology parameters which are reported in Tab.4.1 are realistic for a standard twin-tub CMOS process but they do not refer to a specific technology and in particular, they do not refer to the technology which has been considered for the validation of the models presented in the previous Chapter.

Table 4.1. Default Values of Model Parameters

Parameter	Unit	Default Value
Opamp Circuit		Volt. Foll.
Differential Pair Type		nMOS
$\frac{\mu_{\rm n}C_{\rm ox}}{2}$	μA/V^2	18
Aspect Ratio, $\frac{W}{L}$	–	25
Bias Current, $I_{\rm B}$	μA	10
Parasitic Capacitance $C_{\rm T}$	pF	1
Parasitic Capacitance $C_{\rm gs}$	pF	0.1
CW RFI Frequency	MHz	200
CW RFI Amplitude	mV	500

4.2.1 Opamp Susceptibility Vs. CW RFI Amplitude

On the basis of Expr.(3.100), with reference to the parameters in Tab.4.1, the dependence of the RFI induced offset voltage on the peak amplitude of CW RFI is plotted in Fig.4.6. It can be noticed, in particular, that the RFI induced offset voltage increases quadratically with the peak amplitude of RFI for low RFI amplitudes, according with Volterra series results, while it increases almost linearly for higher values of RFI amplitude.

According with the considerations which have been presented in the previous Section, the amplitude of RFI superimposed onto the voltage follower input terminal is related to the product of common-mode and differential mode RFI superimposed onto the opamp input terminals and the reduction of this product in order to achieve immunity to EMI can be addressed by a proper design of the feedback network and/or by system level EMI suppression strategies.

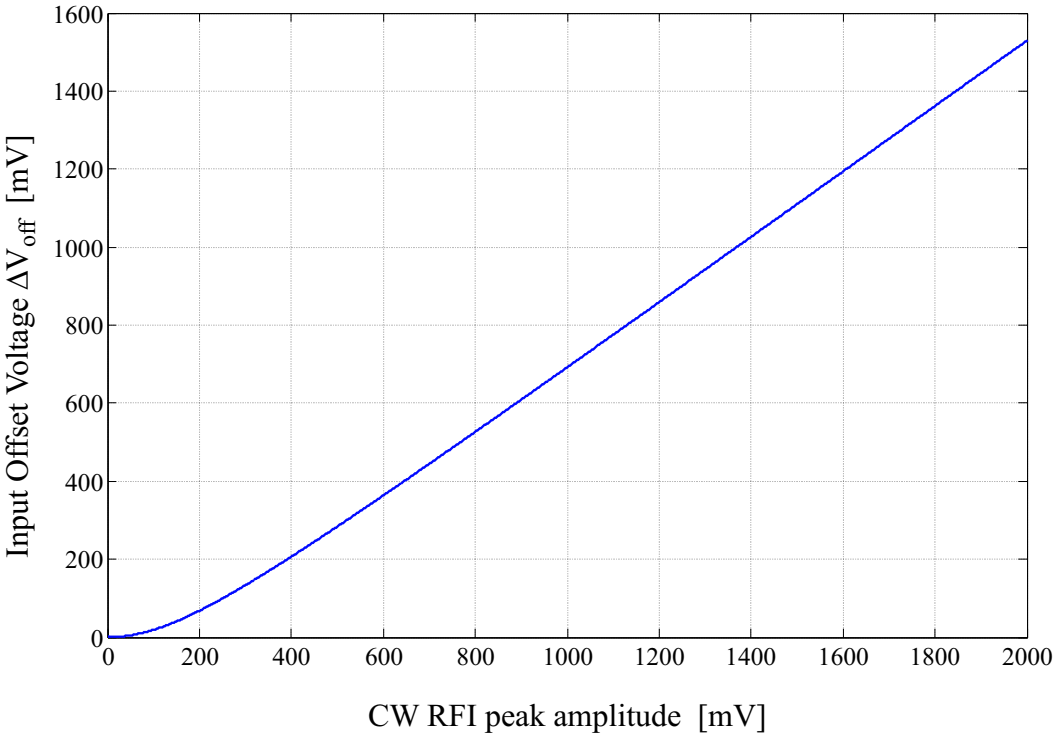


Figure 4.5. RFI-induced Input Offset Voltage versus CW RFI Amplitude.

4.2.2 Opamp Susceptibility Vs. CW RFI Frequency

On the basis of Expr.(3.100), with reference to the parameters in Tab.4.1, the frequency dependence of the RFI induced offset voltage is plotted in Fig.4.6. It can be noticed, in particular, that, at low frequencies, the RFI-induced offset voltage increases with frequency whereas, for higher frequencies, it shows a frequency independent behavior.

From Expr.(3.100), it can be observed that the corner frequency of the response in Fig.4.6 is given by

$$f_{\mathrm{RF}} > \frac{2g_{\mathrm{m}}}{2\pi(2C_{\mathrm{gs}} + C_{\mathrm{T}})}. \tag{4.7}$$

The frequency dependence of the RFI induced offset voltage can be related to the structure of the differential pair: below the corner frequency the differential pair acts as a double source follower stage which drives the common-source node. Above this frequency, i.e. out of the bandwidth of the source follower stage, the RF voltages superimposed onto the gate-to-source voltages of the input transistors M1 and M2 are substantially given by a frequency-independent capacitive voltage partition between the capacitances C_{gs} and C_{T}, in particular,

$$V_{\mathrm{gs1,RF}} = \frac{C_{\mathrm{gs}} + C_{\mathrm{T}}}{C_{\mathrm{T}} + 2C_{\mathrm{gs}}} V_{\mathrm{EXT}}$$

and

$$V_{\mathrm{gs2,RF}} = \frac{C_{\mathrm{gs}}}{C_{\mathrm{T}} + 2C_{\mathrm{gs}}} V_{\mathrm{EXT}}.$$

On the basis of the frequency dependence of the RFI induced offset voltage in Fig.4.6, it can be observed that the distortion mechanism which has been highlighted in (3.100) is intrinsically a high-frequency distortion phenomenon, therefore it strongly influence the susceptibility to RFI of opamp circuits while it is substantially unnoticeable in low-frequency operation.

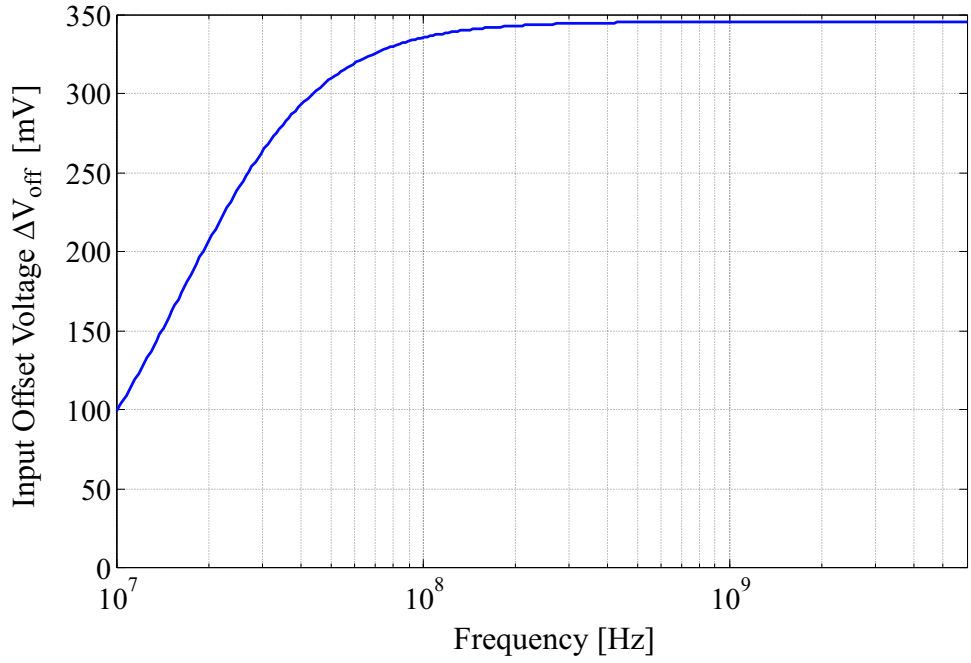


Figure 4.6. RFI-induced Input Offset Voltage versus Frequency.

4.2.3 Opamp Susceptibility Vs. Design Parameters and Parasitic Elements

The influence of design parameters and parasitic elements in the susceptibility to EMI of an opamp circuit is now investigated on the basis of the large-signal closed-form expression of the RFI induced offset voltage derived in (3.100).

According with the results, which have been presented in the previous Chapter, the intrinsic susceptibility of an opamp circuit essentially depends on the RFI distortion of the input differential pair. As a consequence, the analysis which will presented below apply to any opamp circuit topology (Miller, Folded Cascode, Fully differential,...) which include a differential pair as an input stage.

For comparison, the RFI induced offset voltage of an opamp connected in the voltage follower configuration in the presence of CW RFI will be plotted versus the differential pair parasitic elements (parasitic capacitances C_{T} and C_{gs}) and versus its design parameters (bias current I_{B}, input transistor aspect ratio $\frac{W}{L}$). The default values in Tab.4.1 will be employed for the parameters which are kept constant in each plot.

Differential Pair Parasitic Capacitances

The effects of the differential pair parasitics capacitances are now discussed. From Eqn.(3.100), it can be observed that the high frequency distortion induced by RFI in opamp operation depends on the *ratio* $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ and not to the absolute value of parasitic capacitances C_{T} and C_{gs}. According with Eqn. (4.7), in fact, the absolute value of these capacitances is related to the frequency f_{RF} above which the high frequency condition holds.

In Fig.4.8, the high-frequency ($f \gg f_{\mathrm{RF}}$) RFI induced input offset voltage predicted by Eqn.(3.100) is plotted versus the capacitance ratio $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ with reference to the opamp circuit parameters in Tab.4.1. It can be observed that the RFI induced offset voltage increases with $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ and is null if $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}} = 0$, according with the general considerations on the effect of capacitance C_{T} which have presented in the previous Chapter.

The dependence of the capacitance ratio $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ on the differential pair design is now discussed with reference to a nMOS differential pair in an insulated well on the basis of the geometrical considerations, according with the parasitic capacitance extraction methods discussed in [50].

With reference to a nMOS differential pair in an insulated well, the gate-to-source capacitance of one input device is proportional to the gate area

$$C_{\mathrm{gs}} = C_{\mathrm{gs,A}} W L,$$

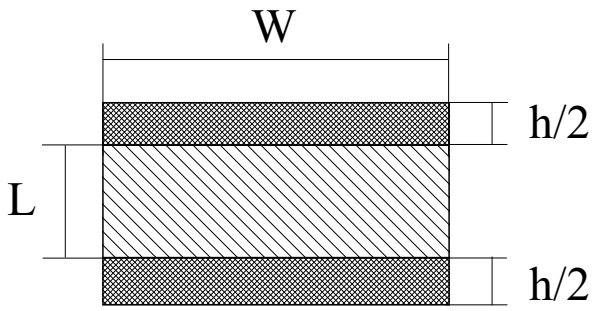


Figure 4.7. Typical MOS Transistor Top View.

where $C_{\mathrm{gs,A}}$ is the gate-to-source capacitance per unit area, while the parasitic capacitance C_{T} is given by

$$C_{\mathrm{T}} = C_{\mathrm{AL,A}} A_{\mathrm{w}} + C_{\mathrm{AL,p}} p_{\mathrm{w}} + C_{\mathrm{db3}} \tag{4.8}$$

where $C_{\mathrm{AL,A}}$ is the well-to-insulation reverse junction capacitance per unit area, A_{w} is the p-well area, $C_{\mathrm{AL,p}}$ is the well-to-insulation reverse junction capacitance per unit perimeter, p_{w} is the p-well diffusion perimeter and C_{db3} is drain-to-body parasitic capacitance of the current source.

If the differential pair is properly laid out in an insulated p-well, the contribution of the first term in (4.8) is dominant and the capacitance C_{T} is substantially proportional to the p-well area. Furthermore, the p-well area is roughly given by the gate area of the two input devices and on the area of their drain and source diffusions therefore, with reference to the typical top view of an MOS transistor in Fig.4.7,

$$A_{\mathrm{w}} \simeq 2WL + 2hW,$$

where h depends on technology. Under these assumptions, the capacitance ratio $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ is given by

$$\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}} = \frac{C_{\mathrm{AL,A}}\,(2WL + 2hW)}{C_{\mathrm{gs,A}} WL} = \frac{2C_{\mathrm{AL,A}}}{C_{\mathrm{gs,A}}} + \frac{2hC_{\mathrm{AL,A}}}{LC_{\mathrm{gs,A}}} \tag{4.9}$$

It can be observed that the second term of Eqn.(4.9) can be reduced increasing the length L of the input devices, whereas the first term of (4.9) only depends on technology and it is not affected by design. Therefore, the capacitance ratio $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ can be reduced increasing the length of the input devices independently of their aspect ratio. For a given aspect ratio, this means a proportional increase in the transistor width and an overall increase in the differential pair silicon area occupation proportional to the square of the scaling factor. Nonetheless, the reduction of $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ which can be achieved by design is limited by the term $\frac{2C_{\mathrm{AL,A}}}{C_{\mathrm{gs,A}}}$ in Eqn.(4.9).

A further reduction in the ratio $\frac{C_T}{C_{gs}}$ can be achieved adding on-chip capacitors in parallel to the intrinsic C_{gs} capacitances. In this case, however, the parasitic capacitances of (floating) on-chip capacitors between their terminals and AC ground (the silicon substrate), could impair their effectiveness. Furthermore, an increase in the input device physical dimensions could be preferable with respect to the connection of on-chip capacitors because it also positively impact MOS opamp performance, as it will be shown in the following. Both the increase in the length of the input devices and the connection of additional capacitors increase the differential pair area occupancy.

The above considerations apply in the case that the parasitic capacitances of the input devices C_{gs1} and C_{gs2} are equal. This is a realistic assumption in practical matched differential pairs, nonetheless, the values of C_{gs1} and C_{gs2} may be intentionally made different in order to enhance the immunity to RFI of a differential pair [45, 46]. In particular, it can be observed from (3.100), that the RFI-induced offset voltage is zero if the peak amplitude of RFI superimposed onto V_{gs1} and onto V_{gs2} are equal. From (3.90), it can be observed that this condition is satisfied independently of the frequency of CW RFI if

$$C_{gs1} = C_{gs2} + C_T. \tag{4.10}$$

Such a condition can be achieved artificially increasing the value of C_{gs1} by connecting an on-chip shunt capacitor. This approach has been proposed by Graffi et al. in [45, 46].

In Fig. 4.9, the effectiveness of this technique is shown on the basis of the model which has been presented in (3.100). This plot shows the RFI induced offset voltage in an opamp circuit connected in the voltage follower configuration in which the parasitic capacitances C_{gs2} and C_T are constant (C_{gs2}=100fF, C_T=1pF) while the capacitance C_{gs1} varies from 10fF to 5pF. It can be observed that when Eqn. (4.10) is satisfied, i.e. when C_{gs1}=1.1pF, the RFI-induced offset voltage is zero.

A limitation of this technique is that the accuracy in the distortion cancellation is related to the absolute value of parasitic elements, therefore the effectiveness of this technique can be impaired by random fluctuations of technology process parameters. Furthermore, the technique which has been discussed above applies specifically to the voltage follower configuration and Eqn.(4.10) should be reconsidered for different opamp-based circuits.

In conclusion, the strong influence of the differential pair parasitic capacitances on the susceptibility to EMI of an opamp circuit has been highlighted and some considerations on the relation between these capacitances and differential pair physical dimensions have been presented. Furthermore, a technique which has been proposed in the literature [45, 46] in order to enhance the immunity to EMI of opamp circuits that is based on the values of differential pair parasitic capacitances has been discussed.

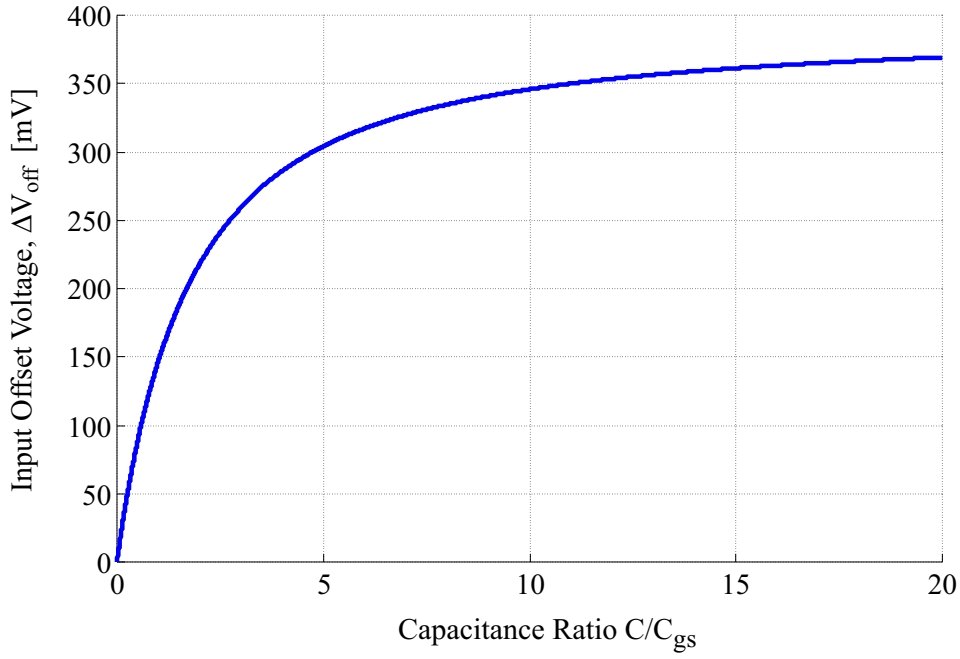


Figure 4.8. RFI-induced Input Offset Voltage versus the Capacitance Ratio $\frac{C}{C_{\mathrm{gs}}}$.

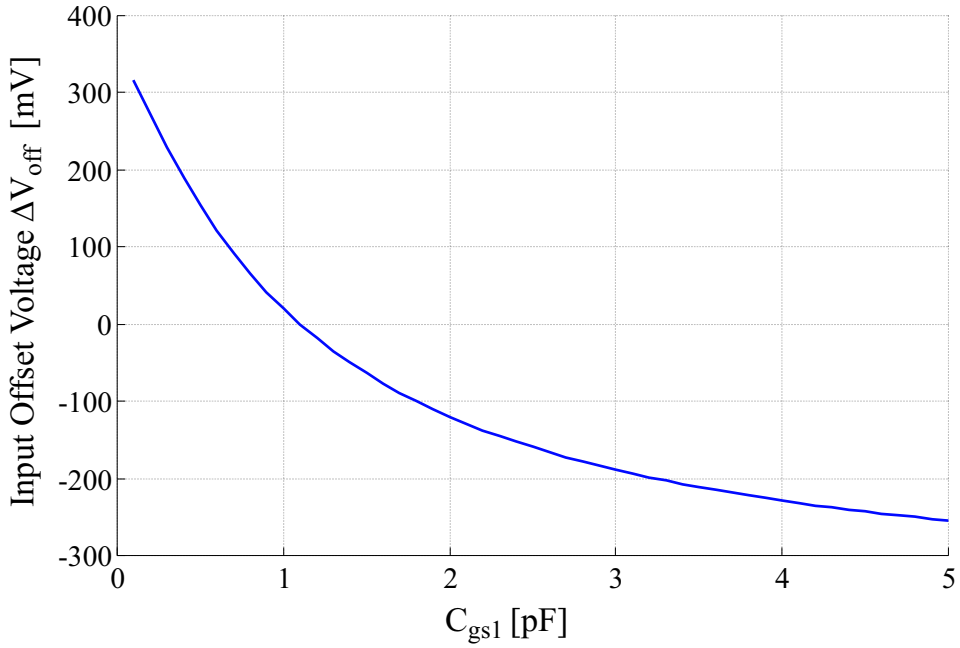


Figure 4.9. RFI-induced Input Offset Voltage versus Parasitic Capacitance C_{gs1}.

Differential Pair Design Parameters

The dependence of the susceptibility to EMI of opamp circuits on the differential pair design parameters is now considered. The nominal design parameters of CMOS differential pairs are the values of the DC bias current I_{B} and the geometrical dimensions of the input transistors channel area (W and L). The impact of the choice of these parameters on the susceptibility to EMI is now investigated on the bases of (3.100).

In Fig.4.10 and Fig.4.11 the RFI induced input offset voltage is plotted versus the differential pair bias current I_{B} and versus the aspect ratio $\frac{W}{L}$ of the differential pair transistors. For the other parameters, the default values in Tab.4.1 have been employed. From these plots, it can be observed that the RFI-induced offset decreases if the input bias current I_{B} is increased while it increases if the aspect ratio of the input devices is increased.

On the basis of these results, it can be observed that the intrinsic susceptibility to EMI of an operational amplifier can be reduced if the input pair bias current is increased and if the input device aspect ratio is decreased. Nonetheless, the choice of these parameters also impacts the performances of the overall opamp circuit, therefore the immunity to EMI should be traded off with other opamp design specifications.

In the following, some of the design tradeoffs which should be considered in order to enhance the immunity to EMI of standard opamp circuits are discussed on the bases of target opamp performances.

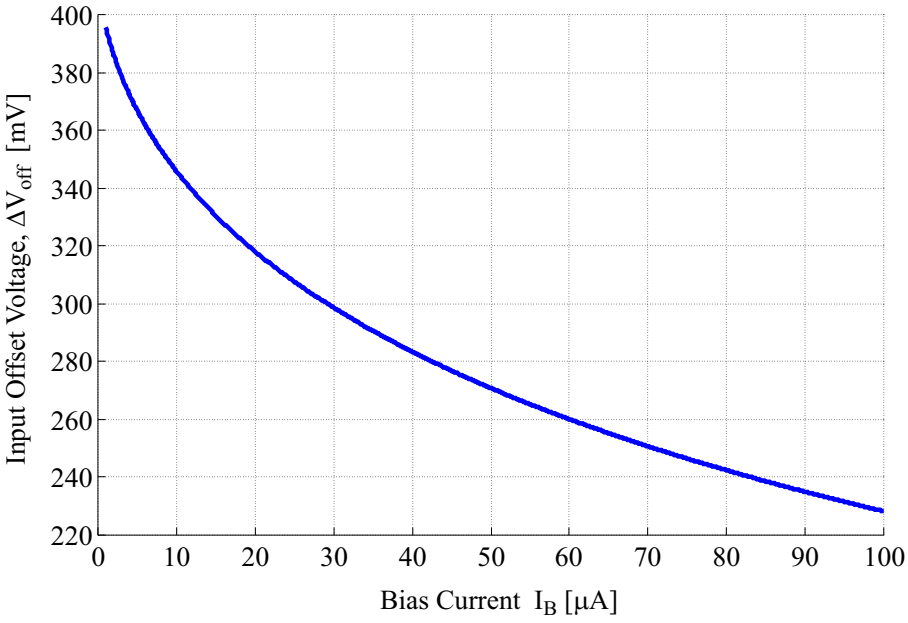


Figure 4.10. RFI-induced Input Offset Voltage versus the Differential Pair Bias Current I_{B}.

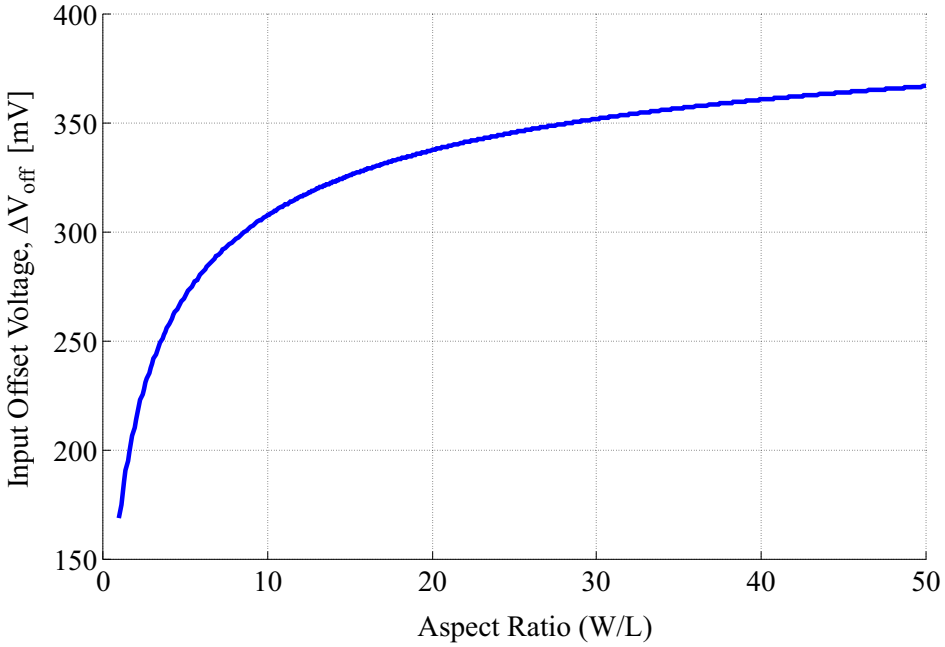


Figure 4.11. RFI-induced Input Offset Voltage versus the Aspect Ratio $\frac{W}{L}$ of the Differential Pair Transistors.

4.3 High Immunity Opamp Design Tradeoffs

The tradeoffs which should be considered in the design of operational amplifiers in order to reduce their susceptibility to EMI are now discussed on the basis of the relationships between RFI-induced offset voltage and differential pair design parameters which have been highlighted in the previous Section.

To this purpose, the standard CMOS opamp design criteria which have been presented in [47] are considered on the basis of Eqn.(3.100) and the relationship between opamp electrical characteristics and susceptibility to RFI is highlighted. In particular, the relationship between EMI susceptibility and differential pair transconductance, differential pair maximum voltage amplification, common-mode voltage input range, static offset voltage, slew rate, bandwidth, power consumption and silicon area occupation are discussed.

4.3.1 Differential Pair Transconductance

A CMOS differential pair acts as a differential-input differential-output transconductance amplifier therefore its nominal in-band operation is described by the small-signal transconductance g_{m} and the small-signal differential output resistance r_{o}. In particular, in circuit topologies where the differential pair drives a low impedance load (e.g. folded cascode opamps) the differential pair transconductance is the main design parameter.

In a CMOS differential pair in which the input MOS devices are biased in the saturation region, the small signal transconductance is given by

$$g_{\mathrm{m}} = \sqrt{2\beta I_{\mathrm{B}}}.$$

In particular, g_{m} depends both on the bias current I_{B} and on the aspect ratio $\frac{W}{L}$ of the input devices, being

$$\beta = \frac{W}{L}\frac{\mu C_{\mathrm{ox}}}{2} = \frac{W}{L}\beta_0.$$

Therefore, the same value of g_{m} can be obtained by different choices of the design parameters I_{B} and $\frac{W}{L}$ and this degree of freedom can be exploited in order to enhance the opamp immunity to RFI.

To this purpose, if a target transconductance $\bar{g}_{\mathrm{m}}$ is required, the input device aspect ratio can be expressed in terms of the bias current as

$$\frac{W}{L} = \frac{\bar{g}_{\mathrm{m}}^2}{2\beta_0 I_{\mathrm{B}}}. \tag{4.11}$$

The above expression for $\frac{W}{L}$ can be employed in Eqn.(3.100) in order to express the RFI-induced offset voltage in an overall opamp circuit in terms of the only bias current I_{B} for a given target transconductance $\bar{g}_{\mathrm{m}}$.

In particular, if the capacitance ratio $\frac{C_T}{C_{gs}}$ is assumed to be independent of the aspect ratio $\frac{W}{L}$ of the input devices[2] and with reference to the model parameters in Tab. 4.1, the opamp RFI-induced input offset voltage has been plotted in Fig.4.12 for different values of the differential pair transconductance g_m.

From this plot, it can be noticed that the RFI-induced offset voltage can be reduced by decreasing the differential pair transconductance g_m and, for a given transconductance, it can also be reduced by increasing the bias current I_B and consequently, by decreasing the aspect ratio of the input devices. In particular, in Fig.4.13, the value of $\frac{W}{L}$ which should be fixed for a given bias current, according with (4.11), is plotted. The decrease in the differential pair transconductance and the increase in the differential pair bias current which are suggested above should be traded off with other design constraints. In particular, from [47], a reduction in the differential pair transconductance negatively affects the opamp performance in terms of static offset voltage and thermal noise, while a increase in the bias current for a constant g_m reduces the opamp common mode input range and increases the power consumption.

[2] A constant $\frac{C_T}{C_{gs}}$ ratio for different aspect ratio $\frac{W}{L}$ of the input devices can be obtained, according with (4.8), by the proper choice of the input device channel length L.

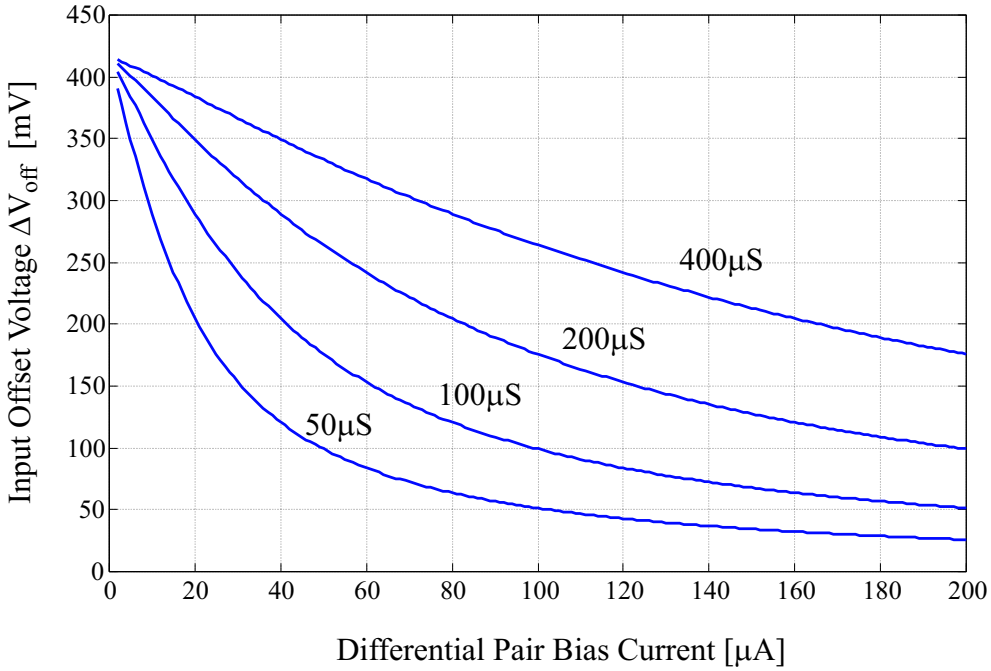


Figure 4.12. RFI-Induced Input Offset Voltage versus I_{B} for different values of the differential pair transconductance g_{m}.

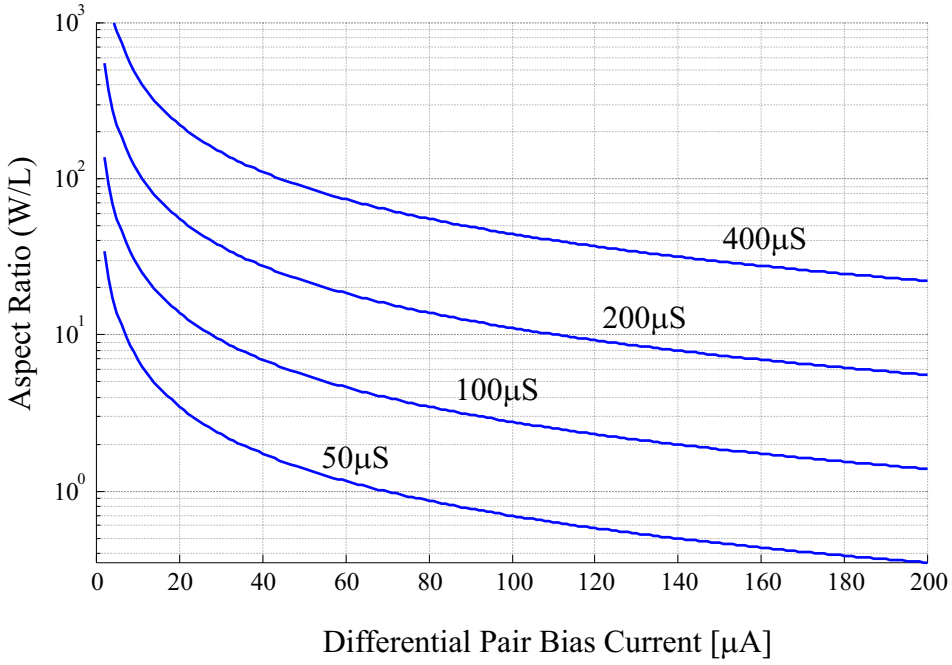


Figure 4.13. Input Devices Aspect Ratio $\frac{W}{L}$ versus I_{B} for different values of the differential pair transconductance g_{m}.

4.3.2 Differential Pair Maximum Voltage Amplification

In opamp circuit topologies where the differential pair drives a high impedance load (e.g., the Miller opamp topology), the output resistance r_o of the differential pair plays a major role in the performance of the stage. In these structures, a differential pair is usually designed to achieve a target maximum voltage amplification

$$A_v = g_m r_o.$$

This parameter express the differential voltage amplification which can be obtained from a differential pair when its differential output is an AC open circuit as shown in Fig.4.14. Furthermore, the maximum voltage amplification is strictly connected with the actual voltage amplification which can be achieved by a differential pair which drives an active load. With reference to the Miller two-stage opamp topology, for instance, the voltage gain of the first stage is given by

$$A_1 = \frac{g_m r_o}{2} = \frac{A_v}{2}.$$

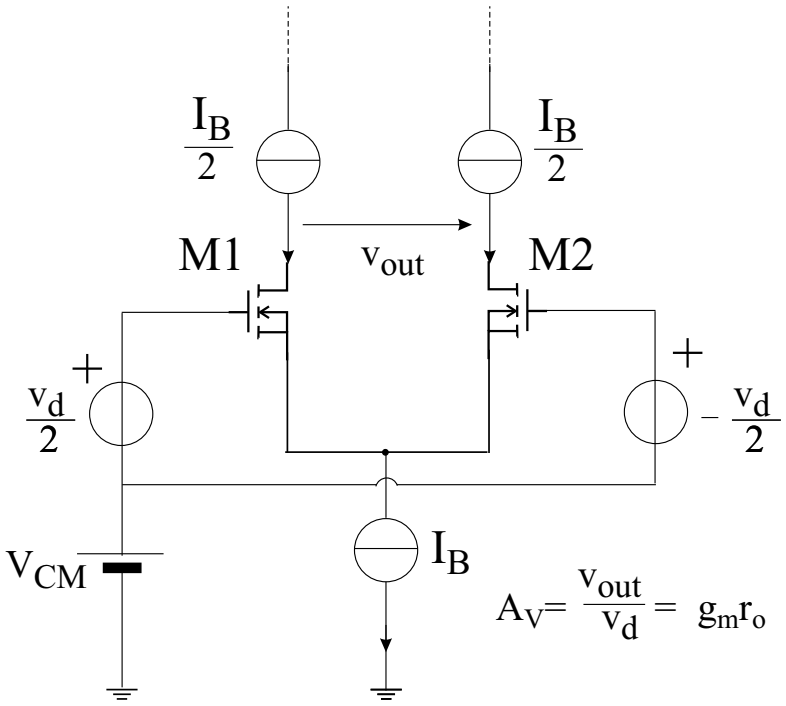


Figure 4.14. Definition of Differential Pair Maximum Voltage Amplification A_v

In a CMOS differential pair where the input MOS devices are biased in the saturation region, the maximum voltage amplification is given by

$$A_{\mathrm{v}} = g_{\mathrm{m}} r_{\mathrm{o}} = \frac{\sqrt{2\beta I_{\mathrm{B}}}}{\lambda \frac{I_{\mathrm{B}}}{2}} = \frac{2\sqrt{2}}{\lambda}\sqrt{\frac{\beta}{I_{\mathrm{B}}}} \tag{4.12}$$

where

$$\beta = \frac{W}{L}\frac{\mu C_{\mathrm{ox}}}{2} = \frac{W}{L}\beta_0$$

and λ is the channel length modulation parameter.

From (3.94) and (4.12) it can be observed that both the maximum amplification A_{v} and the parameter V_{F} which appears in the expression of the RFI induced offset voltage (3.100) depends on $\sqrt{\frac{\beta}{I_{\mathrm{B}}}}$, therefore V_{F} can be directly expressed in terms of the maximum voltage amplification as

$$V_{\mathrm{F}} = \frac{\sqrt{2}}{\lambda A_{\mathrm{v}}}. \tag{4.13}$$

From Eqn.(4.13) it follows that the RFI-induced offset voltage depends on the maximum voltage amplification of the differential pair but, unfortunately, for a given maximum voltage amplification, the immunity to EMI cannot be enhanced trading off I_{B} and $\frac{W}{L}$. In Fig. 4.15 the RFI-induced offset voltage is plotted versus the maximum voltage amplification for different values of the channel length modulation parameter λ, considering the capacitance ratio $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ independent of the aspect ratio $\frac{W}{L}$ of the input devices and employing the technology parameters in Tab.4.1.

Fig.4.15 shows that, for a given maximum voltage amplification, the RFI-induced offset voltage strongly depends on the value of the channel length modulation factor λ. Even thought λ is a technology dependent parameter, it has been shown [48] that this parameter decreases if the length L of the input devices is increased. As a consequence, the opamp immunity to RFI can be enhanced if the channel length of the input devices is increased. In particular, minimum length submicron devices should be absolutely avoided. The increase of the channel length, according with (4.8), also positively impact on the capacitance ratio $\frac{C_{\mathrm{T}}}{C_{\mathrm{gs}}}$ therefore it substantially improve the susceptibility of an opamp to EMI. Nonetheless, the increase in the input device channel implies an increase in the area occupancy of the overall opamp circuit.

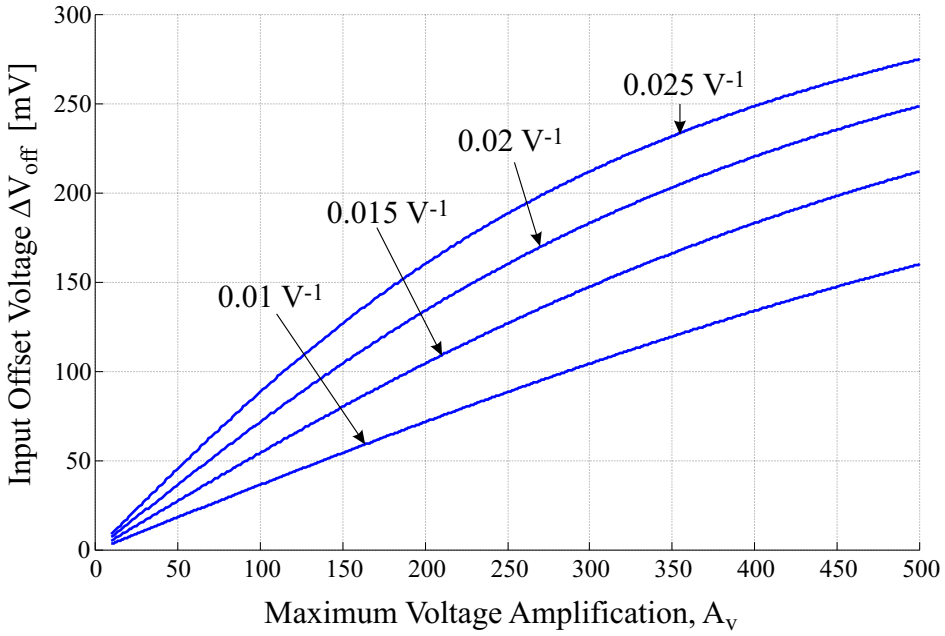


Figure 4.15. RFI-induced Input Offset Voltage versus the Maximum Amplification A_{v} for different values of the channel length modulation parameter λ.

4.3.3 Common-Mode Voltage Input Range

The maximum swing of common mode input signals in opamp circuits has become a primary concern especially in present day low voltage design. In a standard nMOS opamp differential pair, the common mode input range is inferiorly limited by

$$V_{\mathrm{cm,min}} = V_{\mathrm{GS}} + V_{\mathrm{DS3,min}} \tag{4.14}$$

in which $V_{\mathrm{DS3,min}}$ is the minimum drain-to-source voltage to keep the bias current transistor in the saturation region and V_{GS} is the DC value of the input device gate-to-source voltage. In a pMOS differential pair the common mode input range is superiorly limited in a similar way.

With reference to Eqn.(4.14), the value of $V_{\mathrm{DS3,min}}$ is not related to the susceptibility to EMI of an opamp circuit and can be minimized by a proper sizing of the bias current transistor, while the V_{GS} can be expressed as

$$V_{\mathrm{GS}} = V_{\mathrm{T}} + V_{\mathrm{ov}}, \tag{4.15}$$

where V_{T} is the MOS transistor threshold voltage and

$$V_{\mathrm{ov}} = \sqrt{\frac{I_{\mathrm{B}}}{2\beta}}$$

is the overdrive voltage of the input devices. The last term is directly related to the opamp susceptibility to EMI, in fact, the parameter V_{F} in Eqn.(3.100), from (3.94) can be expressed as

$$V_{\mathrm{F}} = \frac{1}{\sqrt{2}} V_{\mathrm{ov}}.$$

Therefore, the common mode input range of a CMOS operational amplifier is directly related to its susceptibility to EMI through Eqn.(3.100). Therefore, the common mode input range must be traded off with the immunity to EMI and, for a given opamp common-mode input range, it is not possible to enhance the opamp immunity to EMI trading off the input device aspect ratio and the bias current. In particular, the RFI-induced offset voltage in the reference opamp circuit in the voltage follower configuration (see Tab. 3.3) is plotted in Fig.4.16 versus the overdrive voltage of its input transistors.

From the above considerations it follows that the immunity to EMI is in contrast with low voltage constraints in standard CMOS opamp design.

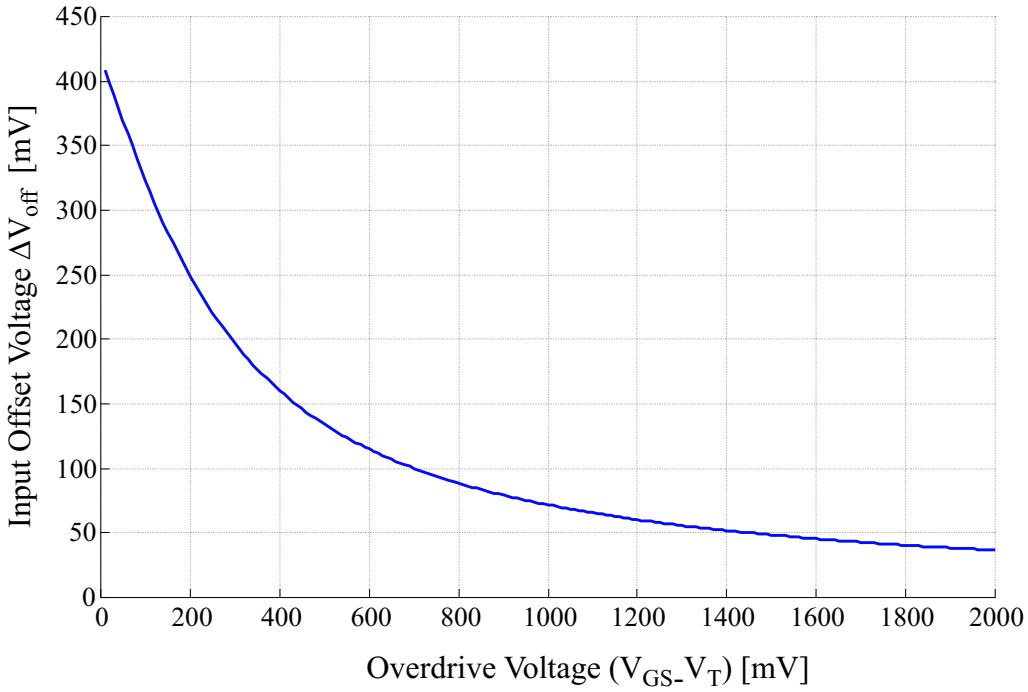


Figure 4.16. RFI-induced Input Offset Voltage versus ($V_{\mathrm{GS}} - V_{\mathrm{T}}$).

4.3.4 Static DC Offset Voltage

The input-referred static DC offset voltage due to differential pair transistor mismatch in an MOS opamp circuit [47], which typically limits the level of accuracy of an MOS opamp in DC applications, can be related to the parameters of its input differential pair as

$$V_{\text{off}} = \Delta V_{\text{T}} + \frac{I_{\text{B}}}{g_{\text{m}}}\delta = \Delta V_{\text{T}} + \frac{(V_{\text{GS}} - V_{\text{T}})}{2}\delta \tag{4.16}$$

where ΔV_{T} is the absolute mismatch in the threshold voltages of the input devices and δ is the relative mismatch in the transconductance parameter β, i.e.

$$\beta_1 = \beta_2 \left(1 + \delta\right).$$

The mismatch in the MOS transistor threshold voltages ΔV_{T} depends on technology and substantially it is not related to design parameters, while the second term in Eqn.(4.16), for a given mismatch in the transconductance parameter, is directly related to the overdrive voltage of the differential pair devices. For this reason, the same considerations on the tradeoffs between immunity to RFI and overdrive voltage which have been presented with reference to the opamp common mode input range apply to the second term in Eqn.(4.16) and its contribution to the static DC offset voltage should be traded off with immunity to RFI, for a given mismatch δ.

Nonetheless, if the mismatch in the transconductance parameters is mainly related to a geometrical mismatch in the aspect ratio of the input devices, which is usually the case in MOS opamps, i.e. if

$$\beta_{0,1} = \beta_{0,2} \qquad \text{and} \qquad \left.\frac{W}{L}\right|_1 = \left.\frac{W}{L}\right|_2 (1 + \delta),$$

it can be observed that the worst-case relative inaccuracy in the aspect ratio is related to the minimum geometrical resolution of a given technology process Δ and to the physical dimensions of the gate area:

$$|\delta| \leq \left|\frac{\Delta}{W}\right| + \left|\frac{\Delta}{L}\right|.$$

Therefore, an increase in both the physical dimensions W and L, for a given aspect ratio $\frac{W}{L}$ may reduce the opamp static DC offset voltage even if the overdrive voltage of the input devices is kept high in order to enhance the opamp immunity to EMI.

4.3.5 Slew Rate Limitation

The design considerations which have been presented before apply to any opamp circuit which employ a differential pair as an input stage. As the slew rate limitation of an opamp circuit i.e., the maximum rate of variation of the output voltage $|\frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t}|$, depends on the structure of the opamp topology and, in particular, on its frequency compensation network, the considerations which are proposed in the following apply to the specific case of a two-stage Miller opamp circuit.

With reference to the two-stage Miller opamp circuit in Fig.3.29 and according with the analysis in [47], the maximum output slew rate can be related to the unity-gain frequency ω_1 and to the input device overdrive voltage as

$$\left|\frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t}\right|_{\mathrm{max}} = \frac{(V_{\mathrm{GS}} - V_{\mathrm{T}})}{2}\omega_1, \tag{4.17}$$

Therefore, with reference to this specific topology, the maximum slew rate is directly related to the overdrive voltage. For this reason, according with the results in Fig.4.16, an increase in the maximum slew rate also improves the Miller opamp immunity to EMI and conversely, the design criteria which should be considered in order to enhance the immunity to EMI of a Miller opamp circuit, positively impact its slew rate transient response.

4.3.6 Opamp Bandwidth

The frequency response of an operational amplifier strongly depends on its internal structure and on its frequency compensation network, therefore it is not possible to relate this parameter only to the design of its input differential pair in a general way.

With reference to the special case of a Miller two-stage opamp circuit [47], whose schematic has been reported in Fig.3.29, it can be observed that the first non-dominant pole, which should be taken into account in frequency compensation as a band-limiting pole, is located at an angular frequency

$$p_{\mathrm{p2}} \simeq -\frac{g_{\mathrm{m2}}}{C_1 + C_2}, \tag{4.18}$$

where C_1 and C_2 are the parasitic capacitances at the output nodes of the first and second gain stages and g_{m2} is the transconductance of the second gain stage, as shown in the small-signal circuit of a Miller opamp in Fig.4.17.

In order to assure closed-loop stability in the voltage follower configuration and to avoid ringing in the opamp step response, the Miller compensation capacitor C_{M} should be chosen in order to fix the opamp open loop unity-gain frequency ω_1

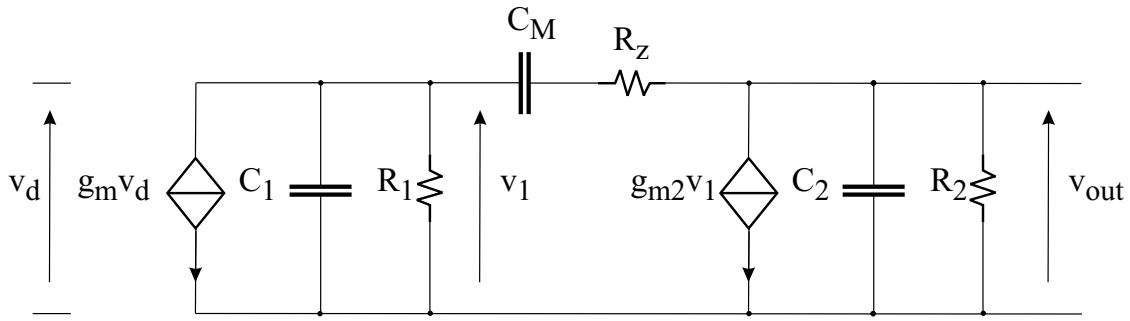


Figure 4.17. Small-signal Circuit of a Two-Stage CMOS Miller Opamp for Frequency Compensation Analysis.

at a frequency which is lower than $|p_{p2}|$, depending on the phase margin which is required. In particular, if

$$\omega_1 = -p_{p2},$$

a phase margin of 45° is achieved [49].

On the basis of these considerations, with reference to the two-stage Miller topology, assuming that C_1 is first order independent of the design parameters of the differential pair, it can be observed that the frequency of the band-limiting pole is substantially independent of the differential pair design parameters, therefore the maximum bandwidth which could be obtained with reference to this topology is not influenced by the differential pair design criteria that should be considered in order to achieve immunity to RFI.

4.3.7 Conclusions

In this Section the main design tradeoff which should be considered in order to enhance the immunity to EMI of standard opamp circuits have been highlighted. In particular, it has been shown that a high immunity to EMI should be traded off with differential pair transconductance, maximum DC voltage amplification, low-voltage constraints and static DC offset performance, while an EMI-robust design is compatible with large bandwidth and high slew rate design.

The results which have been obtained above are summarized in Tab.4.2, which provides a synoptic view of the impact of high immunity constraint on nominal operational amplifier performance.

Table 4.2. Opamp Design Goals and Susceptibility to EMI

Design Goal	RFI immunity
High differential pair g_{m}	-
High maximum voltage amplification A_{v}	- -
High Common mode input range	- -
Low power consumption	- -
Low static DC offset voltage	-
Chip area reduction	- -
High Slew Rate (Miller Opamp)	+ +
Large bandwidth (Miller Opamp)	+

- - should be traded off with immunity to RFI
- can be achieved together with immunity to RFI by design tradeoff
+ independent on the requirements for immunity to RFI
+ + enhanced in a high immunity design

4.4 An Opamp Input Stage Robust to EMI

In the previous Section the optimization of the design of an opamp circuit in order to achieve a high immunity to EMI has been discussed. In particular it has been observed that, in a standard opamp design, a high immunity to EMI should be often traded off with nominal AC and DC performance. In order to overcome this limitation, the standard differential pair should be replaced with opamp input stages which show intrinsically a higher immunity to RFI.

In this Section, on the basis of the insight in the nonlinear mechanisms which has been obtained from the Volterra series models that have been presented in the previous Chapters, a new opamp input stage topology intrinsically immune to EMI is proposed and its operation principle is highlighted. High immunity to EMI of this new structure is compared with standard opamp circuits by computer simulations. The results which are related to this new circuit topology have been published in [51, 52, 53].

4.4.1 Distortion Compensation

From the results about the susceptibility to EMI of opamp circuits which have been shown in the previous Chapter, it has been observed that the sign of the RFI-induced offset voltage in a voltage follower opamp circuit is strictly related to the type of MOS differential pair which is included in it. In particular, nMOS-input opamp circuits are subjected to a positive RFI-induced offset voltage, while pMOS-input opamp circuits show a negative RFI-induced offset voltage, as depicted in Fig.4.18

The key point in the new high-immunity opamp input stage is to exploit these opposite phenomena, that can be evidenced on the basis of the Volterra series analysis which has been proposed in the previous Chapter, in order to achieve a compensation of the RFI induced distortion.

To this purpose, a new opamp input stage which include both a pMOS and a nMOS differential pair has been proposed.

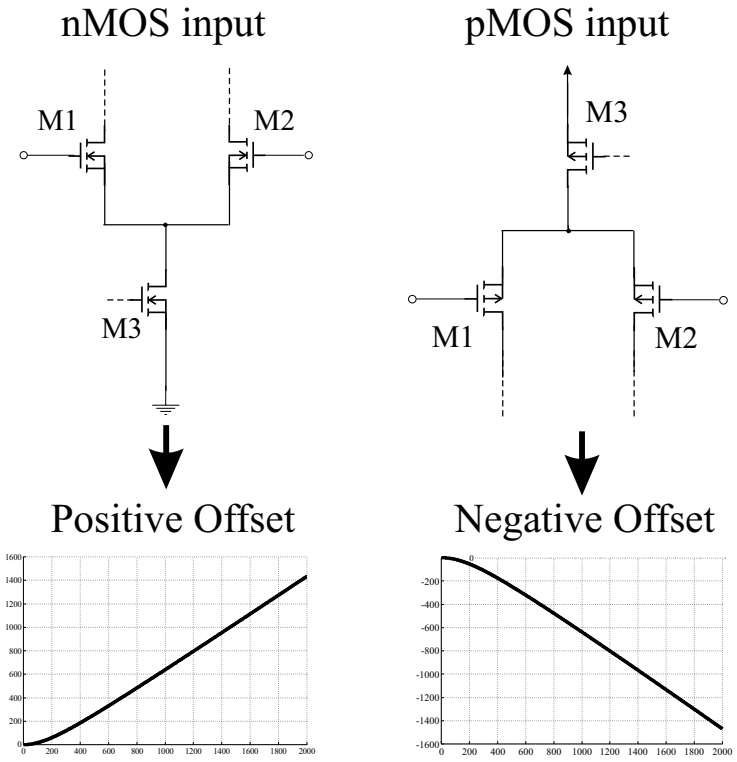


Figure 4.18. Relation between the sign of the RFI-induced offset voltage and the type of differential pair included in opamp circuits

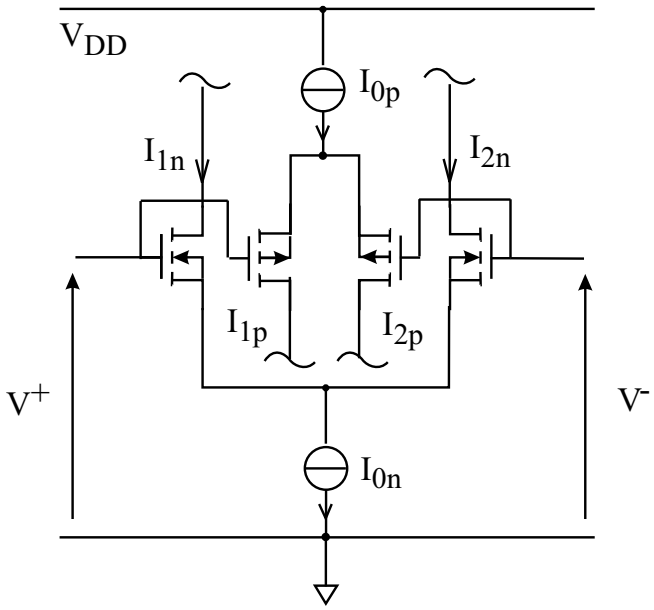


Figure 4.19. Complementary Differential Pair.

4.4.2 Complementary Differential Pair

The high immunity opamp input stage which is proposed is based on the particular distortion compensation mechanisms in complementary differential pairs.

A complementary differential pair is made up of an nMOS differential pair and of a pMOS differential pair whose input terminals are connected together. The output of this structure is the overall differential current, i.e. the sum of the differential currents of each stage[3]

$$I_{\mathrm{D}} = I_{\mathrm{Dn}} + I_{\mathrm{Dp}}. \tag{4.19}$$

Complementary differential pairs, together with a constant transconductance control network, are widely employed in rail-to-rail operational amplifiers [54]: with reference to these circuits, anyway, it has to be pointed out that the distortion compensation discussed in the following requires the operation of both the differential pairs.

[3]The subscripts n and p refer respectively to the nMOS and the pMOS differential pairs.

4.4.3 Complementary Differential Pair Susceptibility to EMI

The susceptibility to EMI of an opamp which include a complementary differential pair as the input stage is discussed on the bases of the two-input Volterra series model which has been presented in the previous Chapter.

To this purpose, it should be highlighted that RFI-induced differential current shift ΔI_{D} in a complementary differential pair, on which ΔV_{off} depends, can be derived from the expressions of the RFI-induced differential current shift in each differential pair which makes up the structure, in fact, from equation (4.19)

$$I_{\mathrm{D}} + \Delta I_{\mathrm{D}} = I_{\mathrm{Dn}} + \Delta I_{\mathrm{Dn}} + I_{\mathrm{Dp}} + \Delta I_{\mathrm{Dn}}$$

and consequently,

$$\Delta I_{\mathrm{D}} = \Delta I_{\mathrm{Dn}} + \Delta I_{\mathrm{Dp}}. \tag{4.20}$$

According with the Volterra series analysis which has been presented in the previous Chapter, the RFI induced offset shift in the differential current of each differential pair can be expressed as

$$\Delta I_{\mathrm{D}} = \frac{g_{\mathrm{p}} V_{\mathrm{d,pk}} V_{\mathrm{cm,pk}} |Y(\mathrm{j}\omega)|}{2} \cos(\varphi_{\mathrm{cm}} + \angle Y(\mathrm{j}\omega)). \tag{4.21}$$

In this expression, $V_{\mathrm{d,pk}}$ and $V_{\mathrm{cm,pk}}$ are respectively the peak amplitudes of the differential and of the common mode component of the input voltage of the differential pair and the term φ_{cm} is the phase shift between the differential and the common mode signals.

The expression for $Y(\mathrm{j}\omega)$ in equation (4.21) is

$$Y(\mathrm{j}\omega) = \frac{2g_{\mathrm{m}}\ \mathrm{j}\omega C_{\mathrm{T}}}{\mathrm{j}\omega\,(2C_{\mathrm{gs}} + C_{\mathrm{T}}) + 2g_{\mathrm{m}}}, \tag{4.22}$$

where

$$C_{\mathrm{T}} = C_{\mathrm{gnd}} + C_{\mathrm{al}},$$

C_{gnd}, C_{al} and C_{gs} are the differential pair parasitics which have been discussed in Section 3.1.4.

Furthermore, according with the analysis which has been presented in the previous Chapter, the input-referred EMI-induced offset voltage in an opamp circuit can be expressed in terms of the RFI-induced offset in the differential current as

$$\Delta V_{\mathrm{off}} = \frac{\Delta I_{\mathrm{D}}}{g_{\mathrm{m}}}$$

where g_{m} is the differential pair transconductance.

On the basis of Eqn.(4.20) and of Eqn.(4.21), the RFI-induced differential current offset in a complementary differential pair is expressed as

$$\Delta I_{\mathrm{D}} = \frac{V_{\mathrm{d,pk}} V_{\mathrm{cm,pk}}}{2} \left[g_{\mathrm{p,n}} |Y_{\mathrm{n}}(\mathrm{j}\omega)| \cos(\varphi_{\mathrm{cm,n}} + \angle Y_{\mathrm{n}}(\mathrm{j}\omega)) + \right. \\ \left. + g_{\mathrm{p,p}} |Y_{\mathrm{p}}(\mathrm{j}\omega)| \cos(\varphi_{\mathrm{cm,p}} + \angle Y_{\mathrm{p}}(\mathrm{j}\omega)) \right] . \tag{4.23}$$

For topological reasons, using for the common mode voltage a sign convention consistent with the proposed model for the RFI induced DC current shift

$$\varphi_{\mathrm{cm,p}} = \varphi_{\mathrm{cm,n}} + \pi \tag{4.24}$$

This expression can be derived on the basis of the small signal circuits of an nMOS and of a pMOS differential pair which are shown in Fig. 4.20. In these circuits the flow of the currents is consistent with the static nonlinear model given in (3.10), i.e. the positive directions of the currents i_{sn} and i_{sp} are consistent with the flow of the DC currents $I_{0\mathrm{n}}$ and $I_{0\mathrm{p}}$.

From Fig. 4.20, it can be observed that an increase in v_{cm} results in an increase of i_{sn} while it results in a decrease of i_{sp}. For this reason, the second order analysis which is proposed is suitable both to nMOS and pMOS differential pairs if the phase convention of expression (4.24) is adopted for the common mode voltages of the two pairs.

On the basis of (4.24), equation (4.24) can be written as

$$\Delta I_{\mathrm{D}} = \frac{V_{\mathrm{d,pk}} V_{\mathrm{cm,pk}}}{2} \left[g_{\mathrm{p,n}} |Y_{\mathrm{n}}(\mathrm{j}\omega)| \cos\left(\varphi_{\mathrm{cm,n}} + \angle Y_{\mathrm{n}}(\mathrm{j}\omega)\right) - \right. \\ \left. - g_{\mathrm{p,p}} |Y_{\mathrm{p}}(\mathrm{j}\omega)| \cos\left(\varphi_{\mathrm{cm,n}} + \angle Y_{\mathrm{p}}(\mathrm{j}\omega)\right) \right] . \tag{4.25}$$

From this expression a nonlinear compensation strategy will be derived in the following.

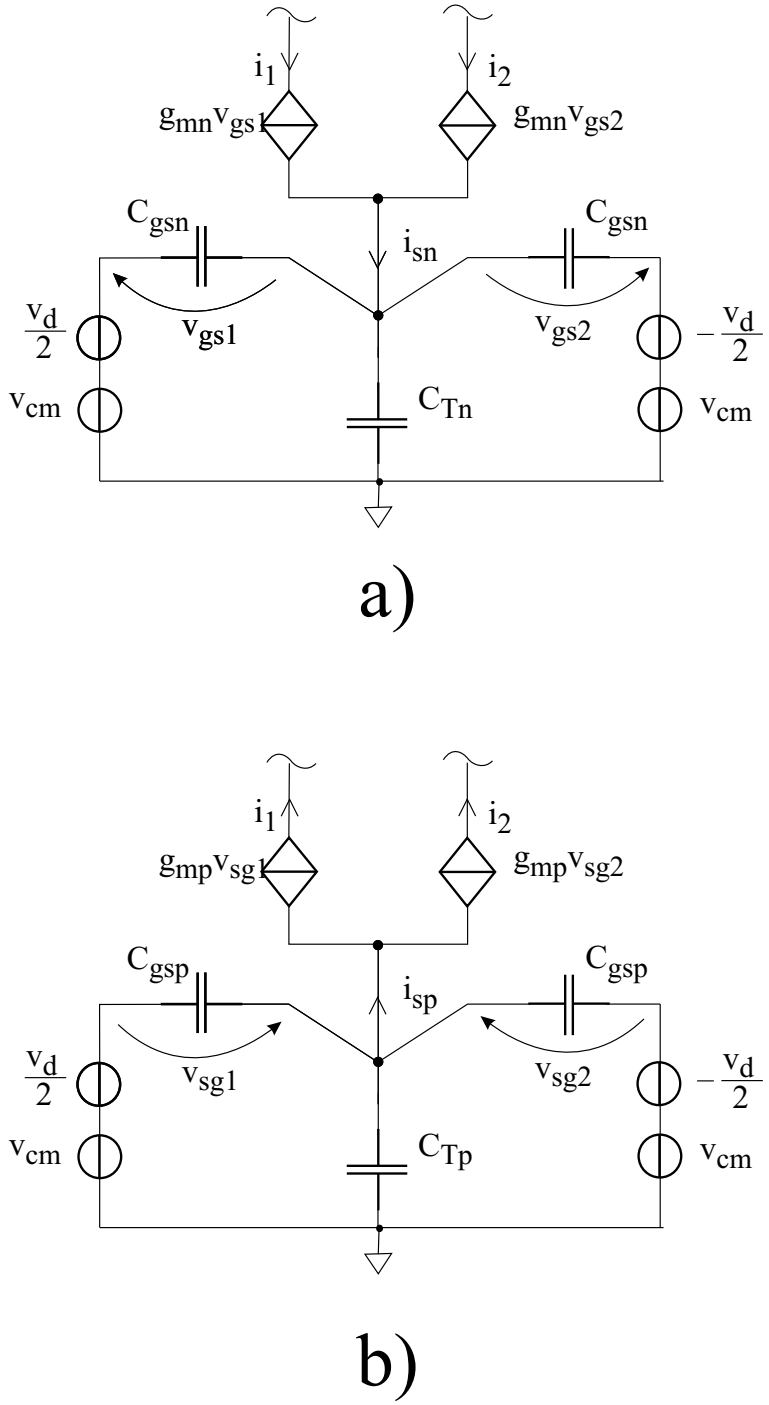


Figure 4.20. Small-signal circuits of a nMOS and of a pMOS differential pair.

4.4.4 Complementary Differential Pair Design

With reference to Eqn.(4.26), it can be noticed how the overall offset current is given by the algebraic sum of two terms with opposite sign, which compensate each other and in particular that if

$$g_{\mathrm{p,n}}|Y_{\mathrm{n}}(\mathrm{j}\omega)|\cos(\varphi_{\mathrm{cm,n}}+\angle Y_{\mathrm{n}}(\mathrm{j}\omega)) = g_{\mathrm{p,p}}|Y_{\mathrm{p}}(\mathrm{j}\omega)|\cos(\varphi_{\mathrm{cm,n}}+\angle Y_{\mathrm{p}}(\mathrm{j}\omega)), \tag{4.26}$$

then

$$\Delta I_{\mathrm{D}} = 0.$$

This nonlinearity compensation mechanism makes complementary differential pairs intrinsically more robust to RF interference than single differential pairs. This higher immunity can be further enhanced by a proper sizing of the stage intended to meet condition (4.26).

Condition (4.26), in particular, can be met for

$$g_{\mathrm{p,n}} = g_{\mathrm{p,p}} \tag{4.27}$$
$$Y_{\mathrm{p}}(\mathrm{j}\omega) = Y_{\mathrm{n}}(\mathrm{j}\omega). \tag{4.28}$$

Furthermore, conditions (4.27) and (4.28) can be met by proper design constrains, in particular condition (4.27) is met choosing

$$I_{0,\mathrm{n}} = I_{0,\mathrm{p}} \tag{4.29}$$

and

$$\beta_{\mathrm{n}} = \beta_{\mathrm{p}}. \tag{4.30}$$

The latter requires

$$\frac{\frac{W}{L}\Big|_{\mathrm{n}}}{\frac{W}{L}\Big|_{\mathrm{p}}} = \frac{\mu_{\mathrm{p}}}{\mu_{\mathrm{n}}}$$

If conditions (4.29) and (4.30) are met, condition (4.28) can be respected for all frequencies if

$$C_{\mathrm{T,n}} = C_{\mathrm{T,p}} \tag{4.31}$$
$$C_{\mathrm{gs,n}} = C_{\mathrm{gs,p}}. \tag{4.32}$$

Conditions (4.31) and (4.32) can be respected adding shunt capacitors in order to compensate the differences in the values of parasitics. For example [15] if $C_{\mathrm{T,p}} > C_{\mathrm{T,n}}$, condition (4.31) can be met adding a shunt capacitor $\Delta C_{\mathrm{T,n}}$ to $C_{\mathrm{T,n}}$ of capacitance

$$\Delta C_{\mathrm{T,n}} = C_{\mathrm{T,p}} - C_{\mathrm{T,n}}.$$

For a given layout, the values of parasitics required can be estimated from process parameters either analytically or by computer simulation (back annotation). Nonetheless, it can be observed that for high frequency CW RFI, the sensitivity of the offset voltage shift to the value of these capacitances is very low.

In fact, for angular frequencies

$$\omega \gg \frac{2g_{\mathrm{m}}}{(2C_{\mathrm{g}s} + C_{\mathrm{T}})},$$

$Y(\mathrm{j}\omega)$, equation (3.9) can be simplified in the form

$$Y(\mathrm{j}\omega) \simeq \frac{2g_{\mathrm{m}}\, C_{\mathrm{T}}}{2C_{\mathrm{gs}} + C_{\mathrm{T}}}, \tag{4.33}$$

and the relative sensitivity of ΔV_{off} to C_{gs} and to C_{T} is given by

$$\frac{\delta \Delta V_{\mathrm{off}}}{\Delta V_{\mathrm{off}}} = \frac{-2C_{\mathrm{gs}}}{2C_{\mathrm{gs}} + C_{\mathrm{T}}} \frac{\delta C_{\mathrm{gs}}}{C_{\mathrm{gs}}} + \frac{2C_{\mathrm{gs}}}{2C_{\mathrm{gs}} + C_{\mathrm{T}}} \frac{\delta C_{\mathrm{T}}}{C_{\mathrm{T}}}. \tag{4.34}$$

For instance, assuming $C_{\mathrm{gs}} = 0.1C_{\mathrm{T}}$, expression (4.34) gives

$$\frac{\delta \Delta V_{\mathrm{off}}}{\Delta V_{\mathrm{off}}} \simeq -0.1 \frac{\delta C_{\mathrm{gs}}}{C_{\mathrm{gs}}} + 0.1 \frac{\delta C_{\mathrm{T}}}{C_{\mathrm{T}}}. \tag{4.35}$$

For this reason, differential pair nonlinear effects can be effectively compensated even though conditions (4.31) and (4.32) are not exactly met and still a high immunity to RFI can be achieved even without adding any shunt capacitor to the circuit.

4.4.5 A High Immunity Operational Amplifier

An operational amplifier based on the high immunity complementary differential pair discussed above has been designed and simulated by ELDO [25], a SPICE-like circuit simulator, using the models of the devices available in the smart power BCD3s [35] technological process.

The proposed structure, which is shown in Fig.4.21 is a standard folded cascode operational amplifier in which the input differential pair has been replaced by the proposed complementary differential pair.

The immunity of this structure to RF interference superimposed onto the input terminals has been verified performing time-domain computer simulations. In particular, the RFI induced offset voltage of the new operational amplifier in the voltage follower configuration has been compared with the RFI induced offset voltage of standard nMOS-input and pMOS-input folded cascode operational amplifiers in the same feedback configuration and under identical test conditions.

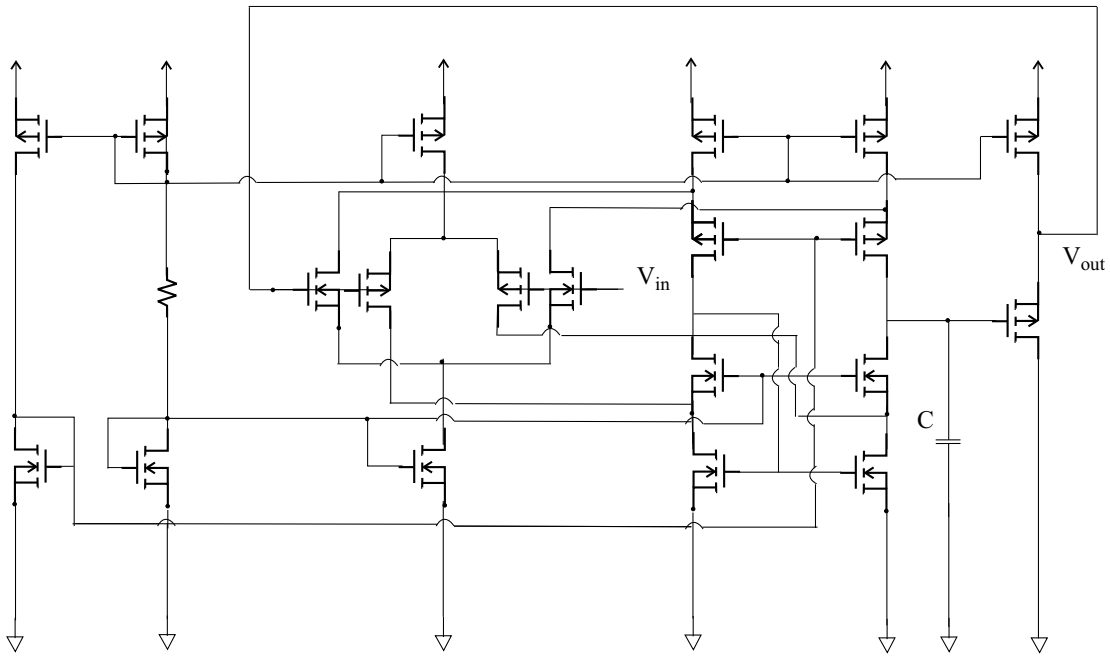


Figure 4.21. High Immunity Folded Cascode Opamp featuring a Complementary Differential Pair input stage.

A plot of the simulated RFI induced DC offset voltage shift in these three structures (High Immunity Complementary Input, nMOS input, pMOS input) is reported in Fig.4.22 as a function of the amplitude of a sinusoidal CW interference superimposed onto the input terminals. In this figure the marks represent simulation results while the solid, dashed and dotted lines represent the prediction obtained by Volterra series analysis.

In Fig. 4.22 it can be noted how effectively the proposed circuit shows particular high immunity features. The residual RFI induced DC offset voltage shift can be ascribed to higher order nonlinear effects neglected in the proposed model.

This model, in particular, is based on the assumption that each transistor is working in the saturation region. If the peak amplitude of the RF interference is high enough, the previous condition is no longer be respected and the offset compensation proposed in this work is no longer effective. Nonetheless, it should be noted that also in these conditions the behavior of the high immunity structure proposed is better than conventional structures.

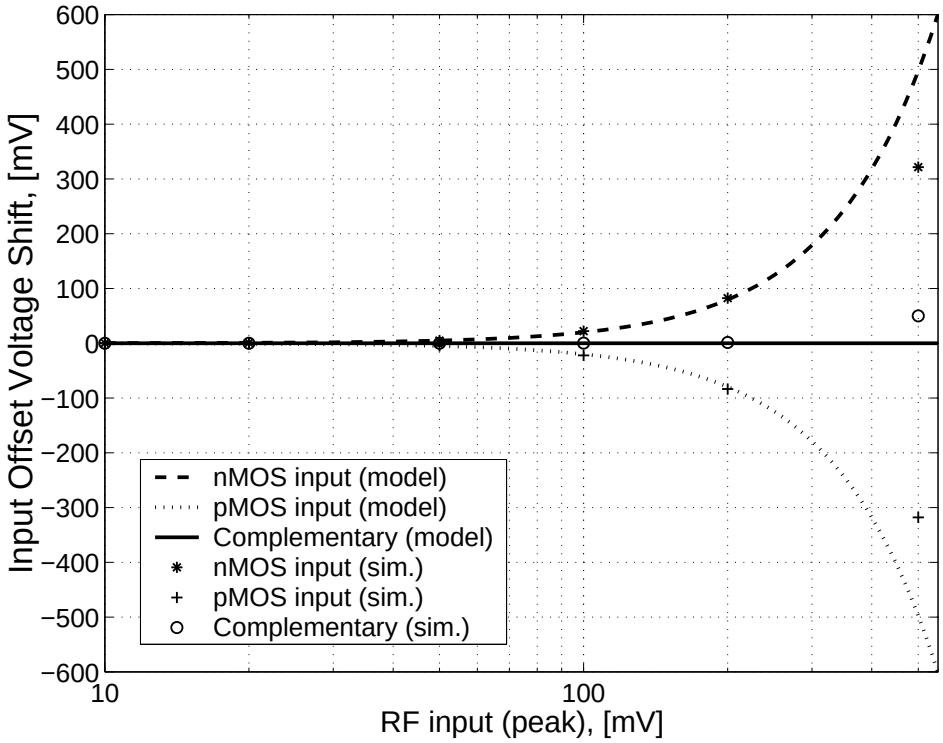


Figure 4.22. RFI-induced offset voltage in the High Immunity Folded Cascode Opamp vs nMOS-input and pMOS-input Folded Cascode Opamps.

4.4.6 Performance Comparison with Standard Design

From the analysis which has been presented above, it can be observed that the complementary differential pair opamp which has been proposed above is intrinsically immune to EMI because of a distortion compensation mechanism. Its intrinsic immunity does not depend, within the validity limits of the model which has been considered, to the absolute values of design parameters and parasitics, therefore the new structure provides a high immunity to EMI independently of other design trade-offs. The design criteria which have been presented above, in fact, do not depend on the absolute value of the design parameters (differential pair bias current and input device aspect ratio) of the nMOS or of the pMOS differential pairs but only on their ratio.

With reference to this structure, in particular, the immunity to RFI should not be traded off with maximum amplification and/or transconductance performance. Nonetheless, it should be noted that, with reference to the new structure, the DC common mode input range is limited both superiorly and inferiorly, according with the requirements of both the nMOS and the pMOS differential pairs. For this reason, it should be noted that the new structure may suffer of limitations in terms of maximum common mode input range.

4.5 EMI-Aware Design of Analog Circuits

In this Chapter, the design of opamp circuit robust to EMI has been systematically addressed, from the effect of the feedback network to the relationship between opamp design parameters, opamp performance and susceptibility to EMI.

The results which have been derived above with reference to opamp-based circuits can be employed in order to enhance the immunity to EMI of analog subsystems which include operational amplifiers. In particular, on the basis of the approach which has been proposed in this work, the susceptibility to EMI of bandgap voltage reference circuits, linear voltage regulator circuits has been investigated. The results of these investigations can be found in the papers [55] and [56].

Furthermore, the criteria and the topologies which have been proposed in this work have been employed in order to enhance the immunity of analog subsystems. According with the design criteria which have been presented in this work, for instance, a Kujik bandgap circuit which operates from a 5V power supply, similar to that which has been presented in the Introduction, has been designed. In Fig. 4.23 the output offset in the reference voltage of this new bandgap circuit is compared with the RFI induced offset in an analogous standard circuit topology. From this plot, the effectiveness of the EMI-aware design criteria which have been presented in this work can be appreciated. In particular, it can be observed that the accuracy of the circuit has been increased by over than two orders of magnitude and the RFI-induced offset voltage is comparable with the nominal thermal drift of the bandgap voltage reference circuits for RFI peak amplitudes up to 1.5V.

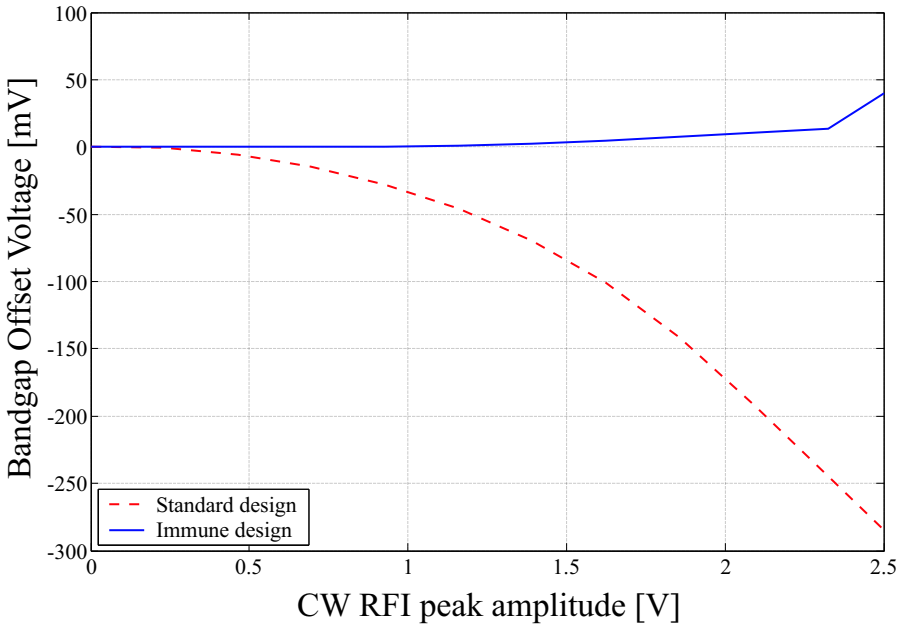


Figure 4.23. RFI-induced offset in the reference voltage of a Kujik bandgap circuits Vs. CW RFI (100MHz) peak amplitude. Dashed line: standard design, continuous line: EMI-aware design.

Chapter 5

Conclusion

In this work the design of analog integrated circuits robust to EMI has been addressed. To this purpose, different analysis techniques which highlight the impact of design parameters and circuit parasitics in the susceptibility of analog integrated circuits have been proposed and these techniques have been employed in order to derive high immunity design criteria and also to develop new circuit topologies for a given analog function with an intrinsic immunity to EMI.

The adverse effects of RFI on the operation of opamp-based analog circuits, in particular, have been investigated and have been related to a high frequency distortion mechanism in the input differential pair. This mechanism is excited by the simultaneous presence of common mode and differential mode RFI superimposed onto the opamp input voltages and it is related to the differential pair parasitic capacitances and especially to the parasitic capacitance between the common-source node and the AC reference voltage. Such a mechanism has been described both qualitatively and quantitatively by two-input Volterra series analysis.

The prediction which have been obtained from the two-input Volterra model of an opamp circuit subjected to EMI have been validated by comparison with experimental test results. To this purpose, a folded cascode CMOS opamp connected in the voltage follower configuration has been designed and integrated with reference to the BCD3s smart power technology and on-wafer CW-RFI direct injection measurements have been performed. With reference to this circuit topology, the predicted and measured RFI-induced offset voltage are in close agreement within the validity limits of Volterra series analysis.

Moreover, Volterra series analysis has been extended to the description of the nonlinear effects which are induced by the presence of RFI superimposed onto the opamp power supply voltage. Even in this case, the susceptibility of opamp circuits has been related to the nonlinear operation of the input differential pair and it has been described by three-input Volterra series analysis. The effect of RFI superimposed onto the power supply voltage, in particular, has been validated by comparison

with on-wafer direct injection experimental results with reference to a folded cascode CMOS opamp connected in the voltage follower configuration. The measured low-frequency intermodulation terms which are added to the opamp output voltage when CW RFI at two different closely spaced frequencies is superimposed onto the voltage follower input terminal and onto the opamp power supply voltage have been compared with model predictions. A good agreement between theory and experimental data has been achieved within the validity limits of Volterra series analysis.

Furthermore, the large-signal analysis technique, which has been proposed by Fiori [20] in order overcome the limitations of Volterra series analysis in terms of amplitude of CW RFI, has been revisited and completed. In particular, a closed-form analytical expression for the RFI induced offset voltage in negative feedback opamp circuits under large signal RFI excitation, which was not provided in [20], has been derived thanks to an *ad hoc* model of the MOS transistor nonlinear operation. Furthermore, thanks to a proper description of RFI propagation within an opamp circuit, the high-frequency RFI assumption in [20] has been removed and a prediction of the frequency dependence of the RFI induced offset voltage under large signal RFI excitation has also been obtained. On the basis of this analysis a single, compact and accurate expression for the RFI-induced offset voltage has been derived.

The predictions of the RFI induced offset voltage which are provided by this models have been compared with on-chip direct injection measurements that have been carried out on three different opamp circuit topologies (pMOS input Miller Opamp, nMOS input Miller Opamp and nMOS input Folded Cascode opamp) connected in the voltage follower configuration and integrated on silicon by the BCD3s multipower technology process. In all the cases, model predictions have proved to be in very close agreement with experimental results even in the case of large signal RFI excitation.

The models which have been developed provide a quite accurate description of the behavior of opamp circuits in the presence of RFI and, in particular, relate RFI-induced distortion phenomena to design parameters and parasitic elements. Such an insight in the nonlinear mechanisms which are responsible of RFI-induced failures in analog integrated circuits has been translated into EMI-aware design criteria.

To this purpose, the effect of the feedback network on the susceptibility to EMI in negative feedback opamp circuits has been firstly investigated. In particular, the RFI propagation in different feedback opamp configurations has been discussed. On the basis of this analysis inverting and non-inverting opamp topologies have been compared and it has been pointed out that the voltage follower opamp circuit is a worst case configuration in terms of susceptibility to EMI.

After the effect of the feedback network has been investigated, the intrinsic susceptibility to EMI of an opamp circuit has been addressed and it has been related to opamp differential pair design parameters and parasitics. To this purpose, the RFI induced offset voltage in an opamp circuit in the voltage follower configuration

has been considered as an EMI susceptibility benchmark and the dependence of this benchmark on differential pair design parameters (bias current and input devices aspect ratios) and parasitic elements (gate to source and common source node to AC ground parasitic capacitances) has been discussed on the basis of the large-signal analytical expression of the RFI induced offset voltage which has been derived.

Moreover, on the basis of the relationship between RFI-induced offset voltage and differential pair design parameters which has been obtained, the tradeoffs which should be considered in the design of operational amplifiers in order to reduce their susceptibility to EMI have been discussed. In particular, standard CMOS opamp design criteria have been revisited on the basis of Eqn.(3.100) and the relationship between opamp electrical characteristics (differential pair transconductance, differential pair maximum voltage amplification, common-mode voltage input range, static random offset voltage, slew rate, input-referred $\frac{1}{f}$ and thermal noise, power consumption, bandwidth and area occupancy) and susceptibility to RFI has been highlighted.

Finally, in order to avoid the tradeoffs between opamp performance and immunity to EMI which have been highlighted, a new opamp input stage topology which is intrinsically immune to RFI has been developed on the basis of the insight in the nonlinear effects which induce RFI distortion in opamp circuits. The proposed new opamp input stage, which includes a complementary differential pair, i.e. a structure which is made up by a nMOS differential pair and a pMOS differential pair, is based on a compensation in nonlinear distortion induced by RFI in nMOS and in pMOS differential pair in order to achieve immunity. The analysis tools which have been previously derived, in particular, have been employed in order to enhance the intrinsic immunity of this structure to achieve a complete cancellation of RFI induced distortion. A high-immunity complementary differential pair has been exploited in the design of a folded cascode operational amplifier and the high immunity of this opamp circuit has been verified by time-domain computer simulations.

The results which have been proposed in this work pave the way to the systematic improvement of the immunity to EMI of a wide class of analog integrated circuits by design. In particular, the tools which have been discussed in this work have been already employed in the analysis of more complex analog circuits like bandgap voltage references and linear voltage regulators and the results of this analysis, which have been published in [55], [56], have brought to the design of a Kujik bandgap circuit which is intrinsically immune to EMI.

Nonetheless, further research effort on the design of analog integrated circuits robust to EMI is required. In particular, some classes of widely employed analog circuits which cannot be reduced to the structure which has been considered in this work require further investigation. Among these circuits, in particular, low-frequency and RF oscillators, PLL circuits and switched capacitor filters should

be considered. Furthermore, on the basis of the insight in the operation of single analog cells, the investigation on the susceptibility to RFI should be extended to data conversion systems as A/D and D/A converters, to power electronic systems as switching power converters and also to digital gates. On the basis of the insight which can be obtained by such an investigation, the same approach which has been adopted in order to relate the electrical performance of a single cell to its susceptibility to EMI can be extended in order to relate the overall susceptibility of a complex system to high-level performance or specifications.

Furthermore, the analysis of the coupling paths which may convey RFI to the input terminals and/or to the power supply rails of analog integrated circuits deserves particular attention. In particular, the effects of substrate coupling in complex multipower circuits and/or the effects of the IC traditional and advanced packaging solutions in the coupling of external electromagnetic fields and/or in the intra-EMC aspects should be investigated. On the basis of this analysis, the amplitude of RFI superimposed onto IC nominal voltages can be expressed as a function of the external incident fields and/or conducted emissions with reference to EMI susceptibility compliance tests and in-field operation, in order to formulate proper chip-level specifications which assure EMC compliance and reliable operation.

In conclusion, the intent which has aimed this research, which dealt with analog circuit and, in particular, opamp-based circuits, should be pursued to its widest extent in order to take EMC issues and tradeoffs to the very first, high level stages of any IC and SoC design.

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